IRPS 2021 Workshops– Circuit Reliability and Aging: Measurements and Simulations

Brief summary: In order to determine the chip performance for a given set of design rules, operating voltage and switching speeds, the reliability must be accounted for specific operating conditions. The question is how to account it in right and most effective way. Should we employ the formal approach treating the circuitry as a sequence of elements characterized by known rates of failures, which are traditionally based on the lab data? Or, should we employ more physics-based description of the failure mechanism of the circuitry as a system in the specific environment?

This workshop focuses on the hot topics in the field of circuit reliability:

1. What has been accomplished so far and what should be the path moving forward?
2. ML based approaches are being explored to establish that. Is this the right approach?
3. Are in situ measurements more appropriate to calibrate the models and close the loop?
4. What is the best approach in addressing the extra challenges coming with 3D integration like thermal and mechanical CPI issues to the whole complexity?
5. How to design a chip with a required functionality and performance while satisfying the intended lifetime of the product?

Workshop organizers

Dr. Valeriy Sukharev (Mentor Graphics)

Valeriy Sukharev is a Technical Lead with the Design to Silicon Division (Calibre), Siemens PLM, Fremont, CA, USA. He has received the Engineer-Physicist Diploma degree in microelectronics from the National Research University of Electronic Technology (MIET), Moscow, Russia and Ph.D. degree in Physical Chemistry from the Russian Academy of Sciences. Prior to Mentor Graphics, Dr. Sukharev was a Chief Scientist with Ponte Solutions, Inc., a Visiting Professor with Brown University, and a Guest Researcher with NIST, Gaithersburg, MD. He also held senior technical positions with LSI Logic Advanced Development Lab. He was a recipient of the 2017, 2019 and 2021 Best Paper Awards from the International Conference on Computer-Aided Design (ICCAD) and the 2016 & 2018 Mahboob Khan Outstanding Industry Liaison/Associate Awards (SRC). His current research interests include development of new full-chip modeling and simulation capabilities for the electronic design automation, semiconductor processing and reliability management. He coauthored the book “Semiconductor Sensors for Physico-Chemical Studies” (Elsevier Science) and edited a number of Proceeding of the series “Stress induced phenomena in metallization” (AIP). He serves on the editorial boards and technical/steering committees of a number of profiling journals and conferences.

Dr. Georgios Konstadinidis (Google)

Georgios K. Konstadinidis is a Technology and Chip Implementation Lead at Google focusing on the R&D of Machine Learning Accelerators. He received a Ph.D degree in electrical engineering from the Technical University of Berlin, Germany and a B.Sc. Degree in Physics, M.Sc. in electronics from the Aristoteles University Thessaloniki Greece. From 2010 to 2017 he was a Senior Hardware Architect at Oracle and prior to that a Distinguished Engineer at Sun Microsystems, focused on high performance microprocessor physical design. He has been involved in the technology, design porting, physical design, reliability, optimization, circuit methodology, signal integrity, timing, and CAD tools for several projects. From 1991 to 1995 he was the leader of the high performance bipolar ICs design team at the R&D Center of SGS Thomson in England and in Catania, Italy. He was involved in the design of several ICs for telecommunications, in device modeling and process optimization. Dr. Konstadinidis holds 13 patents and has several IEEE publications. He served as a member of the ISSCC Digital Program Committee from 2002 to 2007, and as Guest Editor for the IEEE Journal of Solid State Circuits. He is a co-author of the book "Clocking in Modern VLSI Systems", Springer, 2009. He currently serves as TPC member of the IRPS Digital Circuit Reliability and IEDM Systems & Circuit Reliability sub-committees.