Workshop on BTI and HCD

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Bias Temperature Instability (BTI) continues to remain as a crucial reliability concern in CMOS devices. Although it comes in two variants – Negative BTI (NBTI) in PMOS and Positive BTI (PBTI) in NMOS, modern devices with Replacement Metal Gate (RMG) based High-K Metal Gate (HKMG) processes primarily suffers from NBTI while PBTI is negligible.

The physics of NBTI has remained debated, although any model should be able to explain different experiments (as follows) in order to qualify as something meaningful:

- Time kinetics of NBTI during (stress) and after (recovery) DC and AC stress at multiple gate bias (V_G) and temperature (T) – preferably T range covering space to automotive applications, and AC stress at multiple duty cycle and frequency.

- Impact of different processes, such as Nitrogen in gate stack, Germanium in channel, device dimension (e.g. fin length/width), layout, etc., on the time kinetics, Vg and T dependence.

However, from a qualification viewpoint, simple empirical models are sufficient to benchmark foundries or process recipes, although care should be taken that the stress and use conditions are not much different to project to operating conditions. Physical models can provide better estimation of end-of-life NBTI.

Hot Carrier Degradation (HCD) depends on channel length (L_{CH}), drain bias (V_D) and ratio of drain to gate bias (V_D/V_G). Classical worst-case projections approaches, such as mid V_G (I/O devices or nodes >90nm) or V_G=V_D (node <90nm) might be sufficient for foundries or process benchmark. However, accurate aging model dedicated to circuit simulation might require refined models taking into account complex V_G dependencies, HCD-BTI interaction as well as self-heating effects. As a matter of fact, the BTI-HCD interaction can become a crucial issue especially for PMOS devices, if qualification is done at V_G=V_D condition, and the situation can get exacerbated due to self-heating effect in modern devices (FDSOI, FinFET, GAA NSFET) with confined channels.

This workshop would focus on the following:

- Overview of BTI mechanism (~15 mins)

- Overview of HCD mechanism in high and low voltage devices (~20 mins)

- Qualification / test methodologies for HCD and BTI (~ 25 mins)

    - Choice of stress bias (V_G/V_D condition) and AC-DC factor
    - Decoupling of BTI and HCD
    - Impact of self-heating effect (DC vs. AC stress)

Xavier Federspiel received the Ph.D. degree in microelectronics from the Institut National Polytechnique, Grenoble (France), in 2001. Afterwards, he went to work for Delphi Automotive in the failure analysis group. In 2002, he joined Philips Semiconductors (currently, NXP Semiconductors) R&D Laboratories in Crolles (France), where he worked on reliability of interconnects for advanced CMOS technology. From 2007 to 2009, he worked as process integration engineer at Qimonda GmbH, Dresden (Germany). Since 2009, he worked for successively for Dolphin Integration and ST Microelectronics R&D Center in Crolles (France) as front end reliability engineer (2009-2011) and more recently CMOS Reliability team Leader.

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