Advanced 3D Flash Memory Architectures

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Abstract:

In this tutorial, I will briefly introduce the history of various 3D NAND Flash architectures, including BiCS, TCAT, VG, VSAT, and twin-bit cells (SGVC, HC, or split-gate cell). And then I will briefly illustrate the mainstream 3D NAND structure used in mass production, followed by the future directions for 3D NAND scaling. Next, I will introduce the recently developed 3D NOR-type architecture for low-latency high-speed purposes, including vertical-channel split-gate Flash and 3D AND-type architecture. Finally, I will introduce computing--in-memory (CIM) using 3D NAND and 3D NOR.

Biography:

Hang-Ting Lue received his B.S. and M.S. degrees in physics from National Tsing-Hua University (NTHU) in 1997 and 1999, respectively, and Ph.D. degree in electrical engineering from National Chiao-Tung University (NCTU) in 2002. He joined Emerging Central Lab (ECL) in Macronix (MXIC) since 2003. Currently he is the director of emerging memory R&D division. He has authored and co-authored more than 40 papers in the flagship IEDM and VLSI conferences, including numerous highlight papers, and more than 130 accumulated papers in IEEE journals and conferences.

His publications have got >7700 citations. His research interest includes advanced 3D Flash memory devices, 3D memory architectures, computing-in-memory (CIM), neuromorphic computing, reliability physics, and emerging quantum computing devices. He has >100 granted US patents, including several key patents in bandgap engineered SONOS (BE-SONOS), 3D NAND and 3D NOR architectures that are strongly related to mass-production product. He has frequently served the committee member in various semiconductor conferences including IEDM, VLSI, IRPS, SSDM, IMW for years and is now serving as the technical committee member in VLSI since 2011.