Understanding and Challenges of MOL/BEOL TDDB Reliability

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Abstract:

MOL (Middle-Of-Line) and BEOL (Back-End-Of-Line) dielectric reliabilities have become a great importance for advanced semiconductor process technology development and qualifications. Particularly, dielectric thickness variation effect on MOL/BEOL TDDB has become a severe issue to deal with in terms of characterization and lifetime modeling. This tutorial will begin with an introductory review of MOL/BEOL TDDB followed by various topics such as statistical modeling of Tbd (Time-to-Breakdown), thickness variation effect on Tbd, review of voltage acceleration models, requirements of voltage acceleration model validation, consideration for TDDB test device designs and advanced characterization/modeling methods. As supplemental characterization/screening methods of TDDB, ramped voltage stress (RVS) and ramped current stress (RCS) will also be discussed. Both entry-level and experienced TDDB reliability colleagues are strongly encouraged to attend.

Biography:

Andrew Kim is a senior staff for CMOS reliability R&D at Non-volatile memory Solutions Group of Intel Corporation, Folsom, CA. His current focus is BEOL reliability of Cu interconnects. He served as a chair/vice-chair of Dielectric Committee of IRPS2019/2018. Since 1998, he has been working at various companies on semiconductor interconnect reliability, BEOL process integration, electrical fuse design/reliability, TCAD for strained silicon, CMP modeling, gas turbine design and system reliability, etc. He received a B.S. with a minor in Mathematics in 1995 from California State University, Fullerton, CA, M.S. and Ph.D., respectively in 1996 and 2001, from Rensselaer Polytechnic Institute, Troy, NY, all in Mechanical Engineering.