Tutorial Sunday 1:30 – 3:00 PM

Electronic Design Automation (EDA) Solutions for Latch-up Verification in CMOS and HV Technologies

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The verification of latch-up protection networks in CMOS and HV technologies is a difficult challenge. There are several factors including increasing design and process complexity, higher-pin counts, wide operating voltage ranges, and the overall computational difficulties in dealing with large data sets. Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. These checks are typically focused on layout topology. However electrical information for latch-up risk areas throughout the chip is not readily available. While DRC checks are still useful at early design stages, relying on conventional DRC latch-up checking exclusively, poses a significant risk of missing hidden latch-up pitfalls. Consequently, a fully automated latch-up rule checking approach analyzing electrical information is highly desired.

In this tutorial we will review the essential requirements of the latch-up electronic design automation (EDA) verification flow. Then an overview of existing latch-up EDA solutions across the industry will be given. We will introduce generic rules that can be used as basis for a typical latch-up EDA verification flow in CMOS and HV technologies. Finally, recommendations for future EDA tool development and standardization will be provided.

Michael G. Khazhinsky is currently a Principal ESD engineer/designer at Silicon Labs in Austin, Texas. Prior to joining Silicon Labs, he worked at Motorola and Freescale Semiconductors where he was in charge of the TCAD development and ESD/latch-up protection solutions for emerging process technologies, with a focus on ESD-EDA. Michael has M.S.E.E. and M.S. Physics from the Moscow State Institute of Electronic Engineering, and Ph.D. in Physics from Western Michigan University. Michael is the Chair of ESDA Working Group 18 on EDA. Michael has served as a member of the IRPS, IEW, ESREF, EMC and EOS/ESD Symposium Technical Program Committees, as well as a Workshop Chair, Technical Program Chair, Vice General Chair and General Chair of EOS/ESD Symposium. He currently serves on the Technical Program Committees of 2020 International Reliability Physics Symposium, 2020 International ESD Workshop, and 2020 EOS/ESD Symposium. Michael co-authored over 30 papers and gave a number of invited talks on ESD, EDA, process/device TCAD, and photonic crystals. He was a recipient of seven EOS/ESD Symposium and SOI Symposium “Best Paper” and “Best Presentation” awards as well as Industry Pioneer Recognition Award. Michael currently holds eighteen patents on ESD design, with additional patents pending. Michael is a Senior Member of IEEE and the Director of the ESD Association.