Tutorial Monday 10:00 – 11:30 AM

Full chip CDM ESD Verification
Instructor: Melanie Etherton, NXP

While the basic principle of protecting integrated circuits (ICs) from damage caused by electrostatic discharge (ESD) events is pretty simple, the details of implementing a full chip protection strategy that has minimal impact on area and leakage, does not limit the functionality or performance of the circuit it is protecting, and prevents any damage from ESD events that ICs are exposed to can be very challenging. The nature of Charged Device Model (CDM) ESD events, where charges are distributed over the complete IC and package and discharge currents flows through internal circuitry, significantly increases the challenge for designing an ESD robust product. For CDM ESD, every aspect of the IC integration can have an impact on the overall product robustness, including the placement of local CDM protection for domain crossings, the primary ESD protection for power and ground domains and seemingly small details in the power and ground grid implementation. This tutorial provides insight to a complete set of verification strategies that will ensure predictive capabilities for CDM ESD robustness, including complex products with billions of transistors, sensitive analog circuitry and multiple power and ground domains.

Melanie Etherton is a principal engineer at NXP Semiconductors in Austin, Texas where she designs ESD protection for automotive products in advanced CMOS technologies and develops methodologies to ensure full-chip ESD robustness, including new EDA tools. She has almost 20 years of experience in the field of ESD, including her doctoral research work at Robert Bosch GmbH, Germany for her PhD from the Swiss Federal Institute of Technology (ETH Zurich). She has authored and co-authored numerous papers in the field of ESD and holds several patents in that area. Dr. Melanie Etherton has served as TPC Chair, Vice and General Chair of the EOS/ESD Symposium from 2014 through 2016.