YIR Circuit

EDA aspects

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Achieving high level of performance, time to market and high quality as required by automotive, mission critical and cloud computing applications demands accurate analysis scalable to the billion devices in today's chips. In this EDA focused YIR session of Circuit Reliability we will review papers that cover compact reliability models that take into account recovery effects, self-heating, workload, process, voltage and temperature variations, and also combine accuracy and scalability based on a hierarchical analysis approach.. The workload choice to get good coverage is tricky, and ML methods are being employed to help with this problem. These however require training and in situ measurements are used to form the baseline training set. This knowledge can be used to make changes in the microArchitecture to minimize the chip wearout by proper load balancing and more uniform wearout. This session will review some key papers that cover this complex task and help define the future direction of the EDA circuit reliability analysis.