Gate Stability and Robustness of In-Situ Oxide GaN Interlayer Based Vertical Trench MOSFETs (OG-FETs)

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Abstract—Vertical GaN devices are currently studied for application in next-generation power converters, but very little is known about their reliability. This work presents the first analysis on the stability of In-Situ Oxide GaN Interlayer based Vertical Trench MOSFET (OG-FET) submitted to forward gate bias. Based on pulsed measurements, step stress tests and threshold voltage transients we demonstrate the following original results: (i) under forward gate bias, the devices show a good stability up to 6-7 V; (ii) higher stress voltages induce a positive shift of threshold voltage (VTH), which has a logarithmic time-dependence and is ascribed to the injection of electrons in the oxide. (iii) The trapping mechanisms are recoverable; the related kinetics were investigated by means of threshold voltage transients at different temperatures.

Keywords- GaN, power transistor, GaN vertical transistor.

I. INTRODUCTION

GaN lateral high electron mobility transistors (HEMTs) have demonstrated excellent performance for medium power applications (650 V) [1]. However, for high power applications, vertical GaN devices are preferred, since in lateral transistors the breakdown voltage is limited by the gate-drain length, and the peak of the electric field close to the surface. Several different GaN vertical transistors have been reported in literature (CAVET, trench MOSFET, Vertical fin FET, vertically aligned GaN nanowires) [2][3][4][5]. For the normally-OFF In-Situ Oxide GaN interlayer-based vertical trench MOSFET (OG-FET) excellent DC performance was demonstrated while switching performance looked very promising [6][7]. Despite the potential of this new technology, very little is known about its stability.

The aim of this study is to present the first extensive analysis on gate stability of In-Situ Oxide GaN interlayer based vertical trench MOSFET, submitted to pulsed measurements, step stress tests and threshold voltage (VTH) transients.

II. DEVICE DESCRIPTION

The cross section of the device under test is depicted in figure 1 (a). The epitaxial device structure consists of 2 µm heavily doped n+ GaN with a doping density 5 · 10¹⁸ cm⁻³ and 10 µm lightly doped n' GaN layer (Nd-N'A ~ 9 · 10¹⁵ cm⁻³) as drift region grown on a free-standing n' GaN substrate via metal organic chemical vapor deposition (MOCVD). On top of the drift region a 400 nm p' GaN (Mg doped: 3 · 10¹⁹ cm⁻³) and a 200 nm thick heavily doped n+ GaN (Si doped: 5 · 10¹⁸ cm⁻³) have been grown. A 730-nm-deep trench was done in the gate region, a 10-nm-thick unintentional doped GaN layer has been grown to serve as channel, followed by the in-situ growth of 50 nm of Al₂O₃ as gate insulator. The source region was formed by removing the insulator and the GaN interlayer using an inductively coupled
plasma (ICP) process. Ti/Au stack are used as source, gate and drain electrodes. The details of the device fabrication are reported in [6].

Figure 1 (b) shows the $I_DV_G$ plot of a single unit cell: the threshold voltage is 2.72 V (defined as the voltage corresponding to a current level of 10 nA in the forward $I_DV_G$ curve). When the $V_{GS}$ is higher than $V_{TH}$, an electron channel is formed by accumulation and current flows vertically through the n-GaN drift layer.

### III. Procedure Description and Results

To evaluate the stability and dynamic performance of the devices, we carried out a double-pulse $I_DV_G$ characterization. The gate and drain terminals are synchronously pulsed from a quiescent bias point to a measurement point (increasing at each pulse the gate voltage from -1 V to 12 V with the drain voltage at 4 V), while the source is constantly kept at 0 V (Figure 2). The resulting pulsed $I_DV_G$ plot is in Figure 3 (a): each $I_DV_G$ curve corresponds to a quiescent bias point. The quiescent bias points are selected in forward gate (with source and drain at 0 V). A square-wave driving waveform was used, with 5 ms off-time in which the device is submitted to a trapping condition, and 5 µs on time, in the measurement condition, representing a ~0.1% duty cycle. At the beginning of the test, two pulsed $I_DV_G$ curves (light and dark purple curves) are obtained with the quiescent bias point of $V_{GS, Q}=0 \text{ V}$, $V_{DS, Q}=0 \text{ V}$ in order to ensure that the measurement does not influence the results. The positive gate bias induces a positive shift of the threshold voltage (Figure 3 (b)). The threshold voltage is obtained as the voltage at which the drain current reaches the value of $10^{-4} \text{ A}$ and it shows a minimum variation up to $V_{GS}=6 \text{ V}$, indicating a good stability. For higher gate voltages, a substantial increase is observed, indicating the presence of an electron trapping process. Step-stress analysis was carried out to investigate device reliability under positive gate bias (PGB). During the step-stress test, the device was submitted to a constant voltage stress at the gate with drain and source at 0 V and the gate current was monitored. The gate voltage was increased at each step (step = 0.25 V every 120 s) up to failure. After each step of the stress $I_DV_G$ measurements have been performed to monitor the changes in the threshold voltage of the OG-FET.

![Figure 1](image1.png)

**Figure 1.** a) Schematic illustration of the OG-FET: the epitaxial layers (grown on GaN substrate) consist in 2 µm heavily doped n+ GaN followed by a 10 µm lightly doped n- GaN, 400 nm p+ GaN and 200 nm n+ GaN source contact layer. b) Transfer characteristics by sweeping the gate voltage forward and backward: a clock wise hysteresis of $\Delta V_{TH}$ ~ 0.5 V is observed.

![Figure 2](image2.png)

**Figure 2:** Schematic representation of the procedure used for the double pulse analysis (referred to the quiescent bias point of $V_{GS, Q}=6 \text{ V}$, $V_{DS, Q}=0 \text{ V}$).

![Figure 3](image3.png)

**Figure 3.** a) Pulsed $I_DV_G$ curves in semi-logarithmic scale performed by pulsing the gate and drain terminals from a quiescent bias point to a measurement point (at $V_{GS}=4 \text{ V}$) for different quiescent bias points with positive gate voltage ($V_{GS, Q}$ from 0 V to 12 V, $V_{DS, Q}=0 \text{ V}$) and b) plot of threshold voltage variation from the initial value of $V_{TH}$ calculated at $I_{DS}=1 \times 10^{-4}$. The tested device shows a good stability up to 6-7 V, for higher values of $V_{GS}$ an higher positive shift of the threshold voltage is observed. The $I_DV_G$ curves in (a) are noisy in OFF-state due to the pulsed measurement procedure.
trapping period Δt and I_DV_G measurements are performed at the end of each period of trapping. The trapping period Δt is increased at each step from 10 µs to 100 s (Figure 7 (b)). The I_DV_G plot are obtained by applying to the gate terminal a voltage ramp from V_{G,step} = 4 V to V_{G,step} = 12 V, with 4 V applied to the drain terminal for a constant period of 10 µs. The procedure was repeated for different trapping voltages, V_{G,BIAS}. For each value of V_{G,BIAS} a recovery phase was evaluated with all terminals grounded i.e. the same procedure was performed with V_{G,BIAS} = V_{D,BIAS} = 0 V. The phase of recovery occurs some seconds after the end of the trapping phase in which the device is unbiased. The results reported in Figure 8 (a) show that the trapping mechanism has a logarithmic time-dependence.

The model estimated for the trapping is reported by Wolters and Verwey [8]. Once the first electrons are injected in the insulator, they create a repulsive action that slows the trapping of further electrons in the dielectric. The trapping becomes slower and slower, since the capture probability decreases with time and straight lines are obtained in the ΔV_TH versus log(time) plot. The slope of the linear fit of the ΔV_TH during stress (Figure 8 (a) and (c)) increases with the gate bias: for higher positive bias, the trapping mechanism is accelerated. Only a partial fast recovery is observed after few seconds (Figure 8 (b)) and for higher gate bias, the stress phase starts at higher values of V_TH (memory effect) due to the semi-permanent trapping of electrons in the oxide. We evaluated the temperature-dependence by performing the V_TH transients tests at different temperatures.

The measurements were performed sequentially from 35°C to 95°C at one value of gate voltage of trapping (V_{G,BIAS} = 8 V, V_{D,BIAS} = 0 V). After the trapping phase a recovery phase with (V_{G,BIAS} = 0 V, V_{D,BIAS} = 0 V) was performed for each temperature. The results of the threshold voltage variation during the trapping phase (Figure 9) do not show a significant temperature-dependence, indicating that the trapping process is field-limited and not strongly thermally-assisted.

Our interpretation is the following: during the stress/recovery phase, the electrons can tunnel from one trap site to another in the oxide through hopping conduction [9].

Figure 4. Plot of the gate current during each step (+ 0.25 V) of gate bias stress: at low gate voltage of stress up to 10 V no variation in the gate current is induced, for high gate voltage of stress: an abrupt increase of the gate current is observed for V_{G,step} = 14.75 V.

Figure 5. a) Plot of the I_DV_G characteristics performed after each step of the stress. The positive gate bias induces a positive shift of the threshold voltage (b).

Figure 6. Pictorial view of the band diagram when the device is submitted to positive gate voltage: the electrons in the accumulation channel are injected and trapped in the oxide.
Figure 7. a) Conceptual schematic diagram of the threshold voltage transients measurement system including a waveform generator to drive the gate and drain terminals, two power amplifier. The current probe and the oscilloscope to monitor the drain current. b) Schematic representation of the waveforms applied to the gate and drain terminals during the threshold voltage transient measurement: the device is submitted to a trapping condition \((V_{G,BIAS}, V_{D,BIAS})\) for a variable period \(\Delta t\) and after each trapping period the \(I_DV_D\) has been performed sweeping the gate from \(V_{G,start}\) to \(V_{G,stop}\) for 10\(\mu\)s by keeping the drain at \(V_{D,pulse}\).

Figure 8. a) Plot of the threshold voltage variation for different gate voltage \((V_{G,BIAS} = 0 \text{ V, 5 V, 6 V, 7 V, 8 V, 9 V, 10 V, 11 V, 12 V; } V_{D,BIAS} = 0 \text{ V})\) applied during the threshold voltage transient measurement (normalized to the first \(V_{TH}\) value of the trapping phase). b) Plot of the threshold voltage variation during the recovery phase (all terminals at 0 V). The threshold voltage variation during the stress-recovery phase, was calculated at 200 \(\mu\)A of drain current. The value of drain voltage applied during the \(I_DV_D\) measurements is 4 V c) Slope of the linear fit in Fig.(a): the slope increases linearly with the gate bias.

Figure 9. Plot of the threshold voltage variation (normalized to the first value of \(V_{TH}\)) at different temperatures performed with \(V_{G,BIAS} = 8 \text{ V}\). The threshold voltage was calculated at 200 \(\mu\)A of drain current with \(V_{D,pulse} = 4 \text{ V}\).

By increasing the \(V_{GS}\), more and more traps located far from the interface, inside the dielectric, are filled. Under this assumption, hopping conduction is mostly related to the available states rather than to the activation energy in good agreement with the negligible temperature dependence [9]. The partial \(V_{TH}\) recovery and the memory effect suggest the presence of two different mechanisms related to the different position of traps: traps inside the dielectric layer are expected to need longer time to detraps [10].

IV. CONCLUSIONS

In conclusion, by means of double pulse analysis we carried out the first investigation of the mechanisms responsible for the threshold voltage instability of OG-FETs under gate stress. The positive gate bias induces the injection of electrons from the accumulation channel towards the gate dielectric (resulting in a positive \(V_{th}\) shift). With a novel measurement procedure \((V_{TH}\) transient measurements) we estimated the kinetics of the trapping, finding logarithmic trend over time. The detrapping phase under zero bias is instantaneous for low \(V_{GStress}\). The trapping process was found to be field-, rather than thermally-assisted. This work, together with [11]–[13], gives a contribution on understanding the oxide-related mechanisms that affect the performance of MOS power devices.

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REFERENCES


