STT-MRAM

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Background

Current embedded memory such as SRAM and e-Flash memory face serious issues such as large power consumption and small process margin with CMOS logic. To overcome the issues, STT-MRAM becomes one of key solution and its risk mass production has already started from many major foundries. On the other hand, STT-MRAM has some technical challenge, similar to the other memory technologies.

Discussion Topics

In this workshop, we would like to guide the attendees to discuss the potential of STT-MRAM, the technical challenges, such as soft error rate events, including WER (Write Error Rate) and RDR (Read Disturb Rate) errors of STT-MRAM, and issues for its mass production.

Summary

The most interesting topic was how to achieve good endurance and good retention reliability at the same time. MRAM scaling down was considered to be one of the possible solutions since MRAM efficiency tends to keep improving as scaling down continues.

However, etch damage should be avoided in order to take advantage of scaling down, otherwise MRAM degradation might reach untolerable level.

Attendees agree that many companies are already at the point of initiation of mass production stage.

Malicious magnetic attack could be one of the serious issues when MRAM product enters the consumer markets such as hand held device applications.

Magnetic shield or system level assist also needs to be considered for the success of MRAM products.