SiC Power Device Reliability-- Squeezing the most out of SiC chips

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Background

SiC chips have reached an excellent level of performance and reliability and in some areas they already approach the theoretical limits given by the material. Of course, there remain some issues like threshold voltage drift and low channel mobility. However, the real obstacles for the SiC technology originate from the packaging.

SiC is much stiffer than silicon and, thus, soldering and wire bonding provide a significantly lower power cycling capability, if no counter measures are taken. This issue also compromises the high temperature capability of the devices, which usually goes together with enlarged temperature swings.

Another issue is parasitics, i.e. stray inductances and stray capacitances in the package and the surrounding circuitry. Together with the extremely fast switching the SiC chips provide, stray inductances can drive the devices into avalanche or trigger oscillations, which make the devices uncontrollable. Even worse, stray capacitances can cause false triggering, which can lead to a phase shoot through.

Discussion Topics

All this can overstress the SiC chips or can compromise their reliability, although it is rather a packaging than a chip issue. In the workshop, these packaging induced issues (i.e. low power cycling capability and parasitics) and their impact on the device reliability will be discussed.

Summary

"Squeezing the most out of SiC chips" was the motto of a workshop on SiC devices. SiC chips have reached an excellent level of performance and reliability and in some areas they already approach the theoretical limits given by the material. However, packaging related issues turn more and more into obstacles for a better utilisation of the SiC technology. SiC is much stiffer than silicon and, thus, soldering and wire bonding provide a significantly lower power cycling capability. Counter measures are available but increase process complexity and cost just to be on a par with silicon. Package induced parasitics was another topic. The extremely fast switching of SiC chips together with stray inductances can drive the devices into avalanche or trigger oscillations, while stray capacitances can cause false triggering. The about 20 participants agreed widely with these statements, so there was not much dispute. The discussion became a bit livelier when the workshop went on to the long-term subject threshold instability. What is acceptable for circuit designers and what is not? It was again widely agreed that the threshold drift is crucial, while the hysteresis is rather annoying. In any case, there will be surely further discussion at future IRPSs!