IRPS2019 Circuit Reliability Workshop

Reliability Simulation

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Workshop was well-attended (~50 participants) with good participation from the group. There was also a wide variety of expertise and perspectives (circuit designers, EDA experts, product reliability, foundry, etc.)

Background/Motivation:

- Circuit designers need to deal with multiple reliability mechanisms (BTI, HCI, TDDB, EM, fin self-heat, etc.) while meeting challenging product power/performance/cost constraints.
- Most reliability models and designer "rules of thumb" are based on DC device reliability characterization. However circuits behave very differently, leading to a gap in circuit reliability compared to device predictions.
- Circuit reliability is strongly impacted by physical design, signal timing and slopes, etc. CAD flows are needed which capture this level of detail, while running efficiently on large designs.

What are the largest challenges? Consensus is that this is a major challenge, so we should address the largest gaps first. Several attendees pointed to electromigration as the toughest challenge, where there are significant differences in circuit EM and product specifications, and the lack of clear failure specifications. There was a proposal to build and characterize EM benchmark circuits to better understand current EM margins. Other attendees felt that BTI and HCI were the largest gaps, especially when impact of process variation is considered. Special circuits (high-speed analog, high-frequency clock trees) were discussed as key limiters when aging is considered.

Potential solutions include building more reliability information into the library itself and into the Spice models. While this is effective for analyzing individual circuits, it isn't feasible for block-level or product-level reliability validation: top-level CAD flows are needed here. More circuit benchmarks can also be built to study reliability of key circuits and understand whether margins are set correctly. There was some discussion about the challenging nature of the foundry business – foundries are obligated to provide good parts which meet all specifications, so they typically are very conservative with reliability models. Some customers develop their own reliability models to remove this conservatism. CAD vendors have difficulties dealing with the encrypted models from foundries, which make debug of issues very difficult.

Next steps: There was general agreement from the entire group that these circuit reliability challenges/gaps are real and need to be addressed. There was also agreement that discussing this once per year for an hour at IRPS isn't enough. Some suggestions include holding a longer (4 hour?) IRPS "side event" where these topics can be explored in more detail, as well as potential IRPS focus sessions (similar to this year's CAD invited talks) on reliability simulation and circuit reliability flows.