3D NAND

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Background

When we transfer from 2D to 3D NAND technology, one big advantage is less WL/WL coupling. This enables X4 technology with 3D NAND. However, as 3D NAND Flash is expected to see more than 200 stacked layers in the future, technological solutions to ease the scaling challenges are deemed indispensable. The Z-direction pitch (i.e. gate pitch) shall be reduced to maintain a reasonable string length for the sake of current and for ensuring an easier control of the etching profile of the memory hole. The associated implications would be more severe cell-to-cell interference. In additional, for the mainstream CTF-type (charge trapping Flash) 3D NAND, the charge trapping layer is shared among the cells, meaning that the charge lateral migration and the fast charge loss effect will be more profound once the cell-to-cell distance is made shorter. This causes wider cell Vt distribution and it becomes more serious for X4 which requires much tighter Vt distribution. Other undesired consequences include more daunting metal gate filling. This may result in challenge on the performance. Other prospective challenge for 3D NAND is stress/ wafer warpage; as well as polycrystal channel and gate dielectric/interface quality when the stacking is higher.

Discussion Topics

In this workshop, we will focus our discussion on cell interference and charge loss/gain physical mechanism. We may discuss some of the pressing issues and the way going forward.

Summary

Detailed questions and discussions:

1. How many more stacking layer to expect before the cost benefit of 3D NAND is lost?

-The current trend of continuous increase of the layer number does not see a clear showstopper in the sense that the low sensing current is still manageable and stress-induced warpage can be alleviated via proper processing schemes. Meanwhile, 500 is forecast to be the ultimate layer number when the bit cost is no longer scalable.

2. What are the device impacts of charge lateral migration and fast charge loss?

-From a material perspective, there have been a few papers via simulation discussing the possibility of doping the SiN film with proper atoms to alter the electron migration mobility within the film, which could help retard the detrimental effect of charge migration and charge loss.

-From an electric perspective, complicated programming algorithms and patterns can be applied to deal with this effect. As an example, as opposed to the typical full-sequence PGM, coarse-fine based PGM

algorithm combined with WL-iteration is one effective way to tackle the fast charge loss and interference effects.

3. What are other reliability issues 3D NAND might encounter?

-GIDL-induced ERS was raised as one possible concern because cell-to-cell ERS variability has been reported to be significant as it takes a relatively long period of time (ms) to boost the channel potential and cells in the vicinity of CSL/BL junctions tend to exhibit faster ERS performance than those further away from CSL/BL.

-Now that QLC functionality has been demonstrated, quintuple-level-cell seems the next step forward in further pushing the cell density. However, this needs to be achieved along with a more advanced ECC and a better control of cell behavior. No clear sign on how this will proceed at this moment.

-Research institutes have studied the use of channel materials apart from Si in an attempt to enhance the string current in light of the ever-increasing string length. However, most attendees agreed that the feasibility is quite low in the case of non-Si technology. To meet the possible requirement of extremely low sensing current, innovative sensing schemes should be utilized.