Workshop on BEOL and CPI

Moderators:

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Background

For leading edge devices, achieving acceptable interconnect reliability for electromigration and time-dependent dielectric breakdown (TDDB) becomes more challenging with each technology node. For all technologies (even mature technologies), package reliability is always a challenge, especially in automotive applications, where use conditions are at higher temperatures and longer times compared to consumer products. In this workshop, we will discuss the following.

Discussion Topics & Summary

1. Electromigration
    a. 5nm node and beyond; Do we need alternative metals or is Cu good enough?
    "Cu works fine in 7nm. Current design rules are conservative and there is margin." Wafer fab perspective: "We actually don't know how big the margin is". The consensus is that we need Co for 5nm node and beyond. (for lower resistance, as well as longer EM lifetime).
    b. What is the electromigration mechanism in p-type materials such as Ru?
    Good discussion on conduction mechanism of p-type metals.. It is argued that it is not hole conduction in valence band. Rather, it is conduction of electrons with negative effective mass. Ru can change from p-type to n-type upon stress condition. Similarly, the effective charge number Z of Co can also change sign at elevated temperature. Does it matter? we all agree that Ru has improved reliability vs Cu.*
    c. How to account for localized heating effects?
    Thermal cycle induced from self-heating is more of a concern than constant high temperature. It can cause void formation from metal fatigue. Temperature-aware EM check can be used to confirm reliability at high constant temperature. But the temperature gradient may cause additional atomic flux and result in void formation. Hot spot size is also important. Large hot spots are of more concern than small hot spots. But no good definition on how big is big. It also depends on circuit; Low duty cycle circuits are of more concern for thermal cycle effects.
2. BEOL Time-Dependent Dielectric Breakdown (TDDB)
    a. What is the best model to use for TDDB?
    Model lifetime prediction diverges only in low field. Multi-year TDDB stress performed at IBM, IMEC, Suny Poly suggest power law, square root E and lucky electron can fit data. Mechanisms for high E stress and low E stress not necessarily the same. It is believed

that physical mechanism is bond breaking rather than Cu drifting since metal with liner only or Co also has TDDB fail, although it takes longer than Cu.

b. How to account for process variation? (CD variation, line-edge roughness, etc.)
Method to account for process variation varies from company to company. Reconstruction method has been used to account for LER bu may not be applicable to BEOL. Models assume infinite variation which is pessimistic, because in reality distribution is truncated since it is limited by process control spec.

3. Chip-Package Interaction (CPI)
    a. How to relate test structure data to product lifetime predictions, especially considering that most fails are due to extrinsic mechanisms?
    No discussion due to time limit
    b. Is there a way to electrically detect and screen “weak” solder bump structures or “weak” wire bond structures?
    No discussion due to time limit