# FinFET Reliability Workshop Summary

***Moderators:***

- Chetan Prasad (Intel Corp.)
- Souvik Mahapatra (IIT Bombay)

***Background***

FinFET devices have become the workhorses of advanced technology nodes, providing improved electrostatic control and power vs. performance trade-offs compared to their planar counterparts. As a consequence of the 3D nature of these devices, they exhibit a higher inherent physical complexity with respect to the reliability mechanisms. This workshop intends to focus on a list of topics that span transistor aging degradation, self-heating impacts, oxide failures and other associated modes unique to FinFET devices.

***Attendance***

Attendee Count ~ 43 (balanced attendance, with over 30% each from universities and industry).

***Discussion Details***

Moderators introduced themselves and reviewed the list of discussion topics.
A question was raised on whether we should be concerned about how MOL effects are made worse by FinFETs, but no further discussion occurred on this topic.

*Concerns about Translating Aging Results from Device to Circuit Level*

- Concern was expressed that all the "doom and gloom" scenarios were at device level, but many sources were not seeing practical circuit level fallout that matched these negative expectations.
- Circuit resiliency and driver strength: need to be comprehended.
- Tool challenges: there seem to be some limited studies, where teams have taken device degradation statistics and implemented custom models, but there seem to be no clear off the shelf options.
- Impact assessments can be broadly classified into two areas: parametric shift (aging), and non-parametric shift (oxide BD). There are probabilistic models for latter, which is a non-deterministic effect (much more complex to implement in circuit modeling).
- Calibration: Critical to understand how calibration to circuit data is done (experimentally speaking). From simulation perspective, how important is it to know the details of the use conditions.
- Impact difference: SBD for retention flop or SRAM are very different in impact than for RO – ckt failure is very topology dependent. This could open up the option to treat different IP blocks independently – but it wouldn't change device level characterization expectations or efforts. Bridging these two is what is essential.

*Bridging the Gap through a Change in Benchmarks?*

- Considering NAND/NOR characterization (all modes): the results depends on applications; one possibility is to convince foundry customers that such IP blocks would be better benchmarks vs. single devices.

- In-situ monitoring: this is a great option to not need to know the underlying physics, but to instead get empirical data that helps drive the desired lifetime result. Regarding the concerns from Si area/power impact perspective, new techniques exist that are less impactive.
- Performance guys always have a standardized set of benchmarks – could not reliability do the same? Maybe drive it through JEDEC, with an aim to treat digital/analog/AMS/IO/etc. separately.
- Could benchmark circuits that are aligned across the industry help address this? Could in-situ aging monitors themselves be these benchmarks?
- ***Giuseppe LaRosa is the main contact for this, and will try to drive this through his HC spec efforts.***

*Aging from an IP Qualification Perspective*

- Foundry perspective: L1 and L2 qualifications are the standard. L2 tends to stress an integrated vehicle that looks product like (mainly SRAM and some latch chains). However, the challenge is everything is zero fails – which does not allow for any form of model development.
- Foundry response: qualification is not driven by any device level to circuit level translations. The use of SRAM as the integrated vehicle of choice is because it is well established and easy to implement. Realistically, foundries want to do the minimum activity that ensures that the qualification is done.
- HTOL for IP qualification: Lot of design houses rely on HTOL for IP qualification, but the challenge is zero defect sampling. Pre- and post-HTOL characterization is done, but degradation depends strongly on vectors and visibility. Not all patterns show the "right" results.
- All of the above approaches deal with bottoms-up view. A thought was raised to see if a tops-down approach may work. Could we do this with big data analytics and use large IP blocks and multiple vectors to get the translation to device level?
- Other challenges: product IP is owned by the customer and foundries have no access to it (in many cases). Since aging depends on topology, standard vehicles like SRAM may not capture enough.

*Aging in New Market Areas*

- There was some discussion on non-digital constructs: conventional digital/analog aging impacts are better known, but other new areas such as machine learning (ML) and artificial intelligence (AI) could be much more tolerant to failures. Does this signify a new paradigm for how we approach reliability in these areas?
- Response: this is not fundamentally different from certain cases such as wireless buffers, where the air re-transmit rates can define the failure tolerances. Could the ML and AI areas just be treated through a use condition approach, but at a higher level? The core idea would be to reflect the tolerance of AI/ML and the corresponding intolerance of ADAS/FuSa use conditions.
- The above discussion led to the concept of whether the standardization of mission profiles across the industry could be considered as well? The main inputs for this would be from the design customers, but if parity is achieved, it could improve the understanding of envelopes significantly.
- ***Could this be as a branch of JEDEC action?***