UTB SOI Transistor Reliability

Moderators:

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Background

High Power computing and other products are driving towards FINFET based technology solutions in scaled nodes. But market segments targeted towards low power, low cost and RF are eyeing the UTB SOI roadmap for future products. UTB offers similar advantages as FINFET for controlling SCEs but in addition the Vt can be tuned using back bias allowing lower Vmin. UTB specific reliability challenges include optimizing high voltage devices, Hot Carrier induced degradation, modeling and calibrating self-heating during operation and accelerated reliability testing. The role of back bias in reliability needs careful modeling too. One of the many interesting question in UTB SOI is, can back bias be used for minimizing end-of-life degradation to eliminate product failure. It is important to identify which mechanisms benefit from back bias and which are neutral to it. Some of the key challenges which are shared in bulk FINFETs and UTB SOI is variability. Role of time-zero variability versus degradation induced variability also needs to be quantified and modeled.

Discussion Topics

Please join us on Tuesday evening for an exciting discussion on UTB SOI Transistor reliability. We encourage you to bring your energy, thoughts and technical insight to make this workshop a success.

- Discuss failure mechanisms which require careful technology optimization in UTB SOI
- Impact of self-heating on reliability in SOI UTB
- Impact of Back bias on reliability
- Sources of variability at T0 and post stress