Scott Ruth / NXP Semiconductors

"Practical Aspects of Latchup for Low Voltage CMOS: Design Rules, Layout Floor Planning, and Test"

The goal of this tutorial is to cover various aspects of aspects of latchup that are encountered by individuals in the semiconductor industry in a way that provides a common understanding of the phenomenon and the limitations and nuances of test and prevention measures. From a design perspective, layout floor-planning, design rules, and EDA checks will be covered. From a test perspective, standard DC latch-up testing as well as some discussion of transient latch-up testing will be covered. Finally, real world latch-up failures and diagnoses will be presented.

Scott Ruth joined NXP Semiconductors in 2007 and is currently a staff engineer in the Automotive Microcontrollers and Processers Group in Austin, Texas, responsible for ESD protection design for advanced CMOS processes. Prior to joining NXP Scott worked at Philips Semiconductors for 8 years in various capacities in ESD and latchup qualification, characterization, and design. From 2004-2007 Scott was the ESD technical lead from NXP in the Crolles2 Alliance, with partners ST Microelectronics and Freescale Semiconductor. Scott received a B.S. degree in Physics from the University of California at Davis and a M.S. EE from the University of Colorado at Boulder.