Transistor Technology in Future Nodes

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Abstract

With the introduction of FINFETs transistor scaling continues down to 7 NM, which is predicted to be the last optical node. In this talk we will review the current limitation for the different options beyond 10 NM and its implication for reliability. The overview will cover various material and structural challenges that are being investigated to continue further scaling. Papers addressing co-optimization of design along with device scaling will also be discussed.

About the Author

Tanya Nigam is currently a Distinguished Member of Technical staff at GLOBALFOUNDRIES. After obtaining her PhD from IMEC in the area FEOL reliability she joined Bell Labs, Murray Hill. While at Bell Labs she worked on sub 50 nm device solution such as Vertical Replacement Gate. Later she worked on LDMOS reliability and device optimization. In 2005 she moved to Cypress Semiconductors and worked on 65nm technology node. Since 2007 she has been working on all FEOL reliability mechanism. Her current work focus is on defining reliability metric for future nodes and device to product correlation. She has been session chair at IRPS, IEDM and has more than 55 publications and 5 patents.