TABLE OF CONTENTS

Keynote 1
"Transistors and Reliability in the Innovation Era"
Kaizad Mistry, Vice President and Director of Logic Technology Integration, Intel Corporation

Keynote 2
"Hybrid Memory Cube: Achieving High Performance and High Reliability"
Brent Keeth, Senior Fellow, Advanced DRAM Architectures, Micron Technology, Inc.

Session 2A - Joint BEOL Dielectrics/Gate Dielectrics Reliability

2A.1 Impact of Electrode Surface Modulation on Time-Dependent Dielectric down
K.B. Yeap, T. Shen, G.W. Zhang, S.F. Yap, B. Holt, A. Gondal, S. Choi, S.L. Liew, W. Yao and P. Justison, GLOBALFOUNDRIES

2A.2 A Critical Analysis of Sampling-Based Reconstruction Methodology for Dielectric down (BEOL/MOL/FEOL)
E. Wu, J. Stathis, B. Li, B. Linder*, K. Zhao* and G. Bonilla*, IBM Semiconductor Research and Development Center, *IBM Research Division*

2A.3 Intrinisic Reliability of Local Interconnects for N7 and Beyond, K. Croes
A. Leśniewska, C. Wu, I. Ciofi, A. Banczerowska, B. Briggs, S. Demuynck, Z. Tőkei, J. Bömmels, Y. Saad and W. Gao*, imec, *Synopsys, Inc.*

2A.4 Intrinsic Mechanism of Non-Linearity in Weibull TDDB Lifetime and its Impact on Lifetime Prediction
K. Okada, K. Kurimoto and M. Suzuki, TowerJazz Panasonic Semiconductor Co., Ltd.

Session 2B - Failure Analysis

.

2B.1 Self-Heating Characterization of FinFET SOI Devices using 2D Time Resolved Emission Measurements
F. Stellari, K.A. Jenckins, A.J. Weger, B. Linder and P. Song, IBM Watson Research Center

2B.2 Power Debug on Fully Integrated Voltage Regulators (FIVR) Circuitry Introduced Deep Low Power States
Y.-C. Chen, D. Budka A. Gibertini and J. Davis, Intel Corporate Quality Network

2B.3 Effects of Front-End-Of Line Process Variations and Defects on Retention Failure of Flash Memory: Charge Loss/Gain Mechanism
J. Park, M. Lee, H. Kang, W. Ko, E. Choi, J. Im, M. Lee, D. Chung, J. Park, S. Shin and S. Pae, Samsung Electronics Co., Ltd.

2B.4 Time-Integrated Photon Emission as a Function of Temperature in 32 nm CMOS
A.B. Shehata, A. Weger, F. Stellari, P. Song, H. Deslandes, T. Lundquist* and E. Ramsay*, IBM T.J. Watson Research Center, *DCG Systems*

Session 2C - Soft Error

2C.1 Susceptibility of Planar and 3D Tri-Gate Technologies to Muon-induced Single Event Upsets
N. Seifert, S. Jahinuzzaman, J. Velamala and N. Patel, Intel Corporation

2C.2 Muons and Thermal Neutrons SEU Characterization of 28nm UTBB FD-SOI and Bulk eSRAMs
G. Gasiot, D. Soussan, J.-L. Autran, V. Malherbe and P. Roche, STMicroelectronics, *Aix-Marseille University & CNRS, IM2NP*

2C.3 Critical Charge Dependence of Correlation of Different Neutron Sources for Soft Error Testing
H. Mori, T. Uemura, H. Matsuyama, S.-i. Abe and Y. Watanabe**, Socionext, *Japan Atomic Energy Agency, **Kyushu University*

2C.4 Influence of Supply Voltage on the Multi-Cell Upset Soft Error Sensitivity of Dual- and Triple-Well 28-nm CMOS SRAMs
B. Narasimham, J.K. Wang, N. Vedula, S.Gupta, B. Bartz, C. Monzel, I. Chatterjee, B. Bhuva*, R. Schrimpf* and R. Reed*,*

*Broadcom Corporation, *Vanderbilt University*

Session 2D - Interconnect Metallization Reliability

2D.1 A Case Study of Electromigration Reliability -- From Design Point to System Operations
B. Li, P. Muller, J. Warnock, L. Sigal and D. Badami, IBM Systems and Technology Group

2D.2 Mechanisms of Electromigration under AC and Pulsed-DC Stress in Cu/Low-k Dual Damascene Interconnects
M.-H. Lin and A.S. Oates, Taiwan Semiconductor Manufacturing Company, Ltd.

2D.3 An Evaluation of Accelerated Failure Time Models of Stress-Migration And Stress-Induced Voiding Failures Under VIAS
G. Hall and D. Allman, ON Semiconductor

2D.4 Diagnostic Electromigration Reliability Evaluation with a Local Sensing Structure
F. Chen, E. Mccullen, C. Christiansen, M. Shinosky, R. Dufresne, P. Periasamy, R. Kontra, C. Graas, and G. St Onge, IBM Microelectronics

2D.5 Study of a New Electromigration Failure Mechanism by Novel Test Structure
L.D. Chen, B.L. Lin, M.H. Hsieh, C.W. Chang, J.S. Tsai, J.C. Peng, Y.-H. Lee, Taiwan Semiconductor Manufacturing Company

2D.6 Constant Voltage Electromigration for Advanced BEOL Copper Interconnects
B. Tang, K. Croes, N. Jourdan, J. Bömmels, Z. Tokei, I. De Wolf, E. Wilcox and T. McMullen*, imec, *Cascade Microtech, Inc,*

Session 2E - Compound/Optoelectronics

2E.1 Enhancement Mode Gallium Nitride Transistor Reliability (Invited)
A. Lidow, R. Strittmatter, C. Zhou, and Y. Ma, Efficient Power Conversion Corporation

2E.2 Evidence for Temperature-dependent Buffer-induced Trapping in GaN-on-Silicon Power Transistors
M. Meneghini, R. Silvestri, S. Dalcanale, D. Bisi, E. Zanoni, G. Meneghesso, P. Vanmeerbeek, A. Banerjee* and P. Moens*, University of Padova, *ON Semiconductor Westerring*

2E.3 Proton Irradiation-induced Traps Causing V_T Instabilities and RF Degradation in GaN HEMTs
A. Sasikumar, Z. Zhang, P. Kumar, E. Zhang, D. Fleetwood*, R. Schrimpf*, P. Saunier**, C. Le**, S. Ringel and A. Arehart, The Ohio State University, *Vanderbilt University, **Qorvo, Inc.*

2E.4 ESREF Paper HCS Degradation of 5nm Oxide High -Voltage PLDMOS
C. Olk, S. Aresu, R. Rudolf, M. Röhner, W. Gustin, Infineon

2E.5 Trapping Characteristics and Parametric Shifts in Lateral GaN HEMTs with SiO_2/AlGaN Gate Stacks
M. King, J. Dickerson, S. DasGupta, M. Marinella, R.J. Kaplar, D. Piedra, M. Sun* and T. Palacios*, Sandia National Laboratories, *Massachusetts Institute of Technology*

2E.6 Substrate and Temperature Influence on the Trap Density Distribution in High-k III-V MOSFETs
G. Sereni, L. Vandelli, R. Cavicchioli, L. Larcher, D. Veksler and G. Bersuker*, DISMI- University of Modena and Reggio Emilia, *SEMATECH*

Session 2F - Process Integration

2F.1 Performance and Reliability of Strained SOI Transistors for Advanced Planar FDSOI Technology
G. Besnard, X. Garros, A. Subirats, F. Andrieu, X. Federspiel, M. Rafik*, W. Schwarzenbach***, G. Reimbold, O. Faynot and S. Cristoloveanu**, CEA-LETI, *STMicroelectronics, **IMEP-LAHC, ***Soitec*

2F.2 Transistor Aging and Reliability in 14nm Tri-Gate Technology
S. Novak, C. Parker, D. Becher, M. Agostinelli, M. Chahal, M. Liu, P. Packan, P. Nayak, S. Ramey and S. Natarajan, Intel Corporation

2F.3 Systematical Study of 14nm FinFET Reliability: From Device Level Stress to Product HTOL
C. Liu, H.C. Sagong, H. Kim, S. Choo, H. Lee, Y. Kim, H. Kim, B. Jo, M. Jin, J. Kim, S. Ha, S. Pae and J. Park, Samsung Electronics

2F.4 NBTI in $Si_{0.55}Ge_{0.45}$ Cladding p-FinFETs: Porting the Superior Reliability from Planar to 3D Architectures
J. Franco, B. Kaczer, P.J. Roussel, E. Bury, H. Mertens, R. Ritzenthaler, T. Grasser, N. Horiguchi, A. Thean and G. Groeseneken**, imec, *T.U. Wien, **also ESAT, KU Leuven*

2F.5 NBTI in $Si_{0.5}Ge_{0.5}$ RMG Gate Stacks – Effect of High-k Nitridation
P. Srinivasan, J. Fronheiser, S. Siddiqui, A. Kerber, L. Edge, , S. Siddiqui, R.G. Southwick III* and E. Cartier*,, GLOBALFOUNDRIES, *IBM SRDC*

2F.6 Thermal Behavior of Self-heating Effect in FinFET Devices Acting on Back-end Interconnects
C.-W. Chang, S.E. Liu, B.L. Lin, C.C. Chiu, Y.-H. Lee and K. Wu, Taiwan Semiconductor Manufacturing Company

Session 3A - BEOL Dielectrics

3A.1 A Method for Rapid Screening of Various Low-k TDDB Models
F. Chen, C. Graas, M. Shinosky, C. Burke, K.D. Feng, C. Bosch and R. Muralidhar, IBM Microelectronics, *IBM T.J. Watson Research Center*

3A.2 An Investigation of Dielectric Thickness Scaling on BEOL TDDB
T. Shen, W. Zhang, K.B. Yeap, J. Tan, W. Yao and P. Justison, GLOBALFOUNDRIES

3A.3 On the Voltage Dependence of Copper/Low-K Dielectric down
S.-C. Lee and A.S. Oates, Taiwan Semiconductor Manufacturing Company

3A.4 An Investigation of Capacitance Aging Model for Extreme Low-K and High-K Dielectrics
M.N. Chang, Y.-H. Lee, S.Y. Lee, C.C. Chiu, D. Maji and K. Wu, Taiwan Semiconductor Manufacturing Company, Ltd.

3A.5 TDDB Improvement of Copper/Dielectric in the Highly-Integrated BEOL Structure for 28nm Technology Node and Beyond
C.-P. Chiu, Y.-C. Liu, B.-S. Tsai, Y.-J. Wang, Y.-S. Lin, Y.-R. Chen, C.-L. Weng, S.-Y. Hsueh, J. Hung, H.-Y. Lai, J.-M. Chen, A.H.-B. Cheng and C.-C. Huang, United Microelectronics Corporation

Session 3B - Transistor Reliability Physics

3B.1 Characterization of Time-dependent Variability using 32k Transistor Arrays in an Advanced HK/MG Technology
P. Weckx, B. Kaczer, C. Chen**, J. Franco*, E. Bury, K. Chanda**, J.Watt**, P. J. Roussel*, F. Catthoor and G. Groeseneken, Katholieke Universiteit Leuven, *imec, **Altera Corp.*

3B.2 Transistor Reliability Variation Correlation to Threshold Voltage (Invited)
S. Ramey, M. Chahal, P. Nayak, S. Novak, C. Prasad and J. Hicks, Intel Corporation

3B.3 Impact of RTN on Stochastic BTI Degradation in Scaled Metal Gate / High-k CMOS Technologies
A. Kerber, GLOBALFOUNDRIES Inc.

3B.4 Time Dependent Variability in RMG-HKMG FinFETs: Impact of Extraction Scheme on Stochastic NBTI
A. Chaudhary, B. Kaczer, P.J. Roussel*, T. Chiarella*, N. Horiguchi* and S. Mahapatra, IIT Bombay, *IMEC*

3B.5 Origins and Implications of Increased Channel Hot Carrier Variability in nFinFETs
B. Kaczer, J. Franco, M. Cho, T. Grasser, P. Roussel, S. Tyaginov*, M. Bina*, Y. Wimmer*, L.-M. Procel**, L. Trojman**, F. Crupi***, G. Pitner^, V. Putcha, P.Weckx, E. Bury, Z. Ji^^, A. De Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken and A. Thean, imec, *TU Wien, **USFQ, ***University of Calabria, ^visiting imec from Stanford University, ^^visiting imec from Liverpool John Moores University*

Session 3C - Electronic Systems Reliability

3C.1 Managing Performance-Reliability Tradeoffs in Multicore Processors
W. Song, S. Mukhopadhyay and S. Yalamanchili, Georgia Institute of Technology

3C.2 Maximum Operating Voltage (V_{MAX}) Limit for SOCs in Thin Form Factor Mobile Devices with Touch Sensitive Displays
K. Maitra, T. Ngyuen, K. Srinivas, S. Chen, V. Jadhav, B. Langendorf, J. Purtell, R. Jensen, R. Gannamani, A. Marathe and R. Master, Microsoft Corp.

3C.3 Platform Qualification Methodology: Face Recognition
G. Antanius, R. Trivedi and R. Kwasnick, Intel Corporation

3C.5 Mitigating "No Trouble Found" Field Returns
A. Haggag, N. Sumikawa, A. Shaukat, J. Lee, N. Aghel* and C. Slayman*, Freescale Semiconductor Inc., *Cisco*

Session 3D - Circuit Aging/Circuit Reliability

3D.1 Connecting the Physical and Application Level Towards Grasping Aging Effects
H. Amrouch, J. Martin-Martinez, V.M. van Santen, M. Moras*, R. Rodríguez*, M. Nafria* and J. Henkel, Karlsruhe Institute of Technology, *Universitat Autonoma de Barcelona*

3D.2 Localized Thermal Effect of Sub-16nm FinFET Technologies and its Impact on Circuit Reliability Designs and Methodologies
Y. Sun, C. Zhan, J. Guo, Y. Fu, G. Li and J. Xia, Hisilicon Technologies Co., LTD.

3D.3 Circuit Delay Variability Due to Wire Resistance Evolution Under AC Electromigration
V. Mishra and S. Sapatnekar, University of Minnesota

3D.4 Stochastic and Topologically Aware Electro-migration Analysis for Clock Skew
P. Jain, S.S. Sapatnekar and J. Cortadella**, Qualcomm Technologies Inc., *University of Minnesota, **Universitat Politècnica de Catalunya*

Session 3E - Compound/Optoelectronics

3E.1 Higher Performance and Improved Reliability: Key to Making Photovoltaics the Mainstream Sustainable Electricity Generation Source of the 21st Century (Invited)
J. Poortmans, E. Voroshaszi, W. Deceuninck and J. Szlufcik, imec, *University Hasselt*

3E.2 Degradation Mechanisms of Dye-Sensitized Solar Cells: Light, Bias and Temperature Effects
A. Cester, N. Wrachien, M. Bon, G. Meneghesso, R. Bertani, R. Tagliaferro, S. Casolucci*, T.M. Brown*, A. Reale* and A. Di Carlo*, Padova University, *University of Rome "Tor Vergata"*

3E.3 Stress-Induced Instabilities of Shunt Paths in High Efficiency MWT Solar Cells
M. Barbato, M. Meneghini, A. Cester, A. Barbato, E. Zanoni, G. Meneghesso, G. Mura, D. Tonini**, A. Voltan** and G. Cellere**, University of Padova, *University of Cagliari, **Applied Materials Italia S.r.l.*

3E.4 Negative Bias Instability in 4H-SiC MOSFETS: Evidence for Structural Changes in the SiC
M. Anders, P. Lenahan and A. Lelis, Penn State University, *US Army Research Laboratory*

Session 3F - ESD/Latch-up

3F.1 ESD Characterization of Planar InGaAs Devices
Z. Ji, D. Linten, R. Boschke, G. Hellings, S.H. Chen, A. Alian, D. Zhou, Y. Mols, T. Ivanov, J. Franco, B. Kaczer, X. Zhang*, R. Gao*, J. Zhang*, W. Zhang*, N. Collaert and G. Groeseneken, IMEC, *Liverpool John Moores University*

3F.2 Improved GGSCR Layout for Voltage Overshoot Reduction
Z. Chen, R. Mertens, C. Reiman and E. Rosenbaum, University of Illinois at Urbana-Champaign

3F.3 Methodology to Achieve Planar Technology-Like ESD Performance in FINFET Process
J.-H. Lee, M. Prabhu, K. Korablev, J. Singh and M. Iyer Natarajan and S.M. Pandey, GLOBALFOUNDRIES Inc.

3F.4 A Novel 8kV On-Chip Surge Protection Design in xDSL Line Driver IC
S.-F. Hsu and J.-Y. Jao, MediaTek Inc.

Session 4A - Transistor Reliability Physics

4A.1 Characterization and Reliability of III-V Gate-all-around MOSFETs (Invited)
M. Si, S. Shin, N. Conrad, J. Gu, J. Zhang, A. Alam and P. Ye, Purdue University

4A.2 Delay Effects and Frequency Dependence of NBTI with Sub-microsecond Measurements
Y.-C. Huang, M.-H. Hsieh, T.-Y. Yew, W. Wang, D. Maji, Y.-H. Lee, W.-S. Chou, P.-Z. Kang, Taiwan Semiconductor Manufacturing Company

4A.3 Combined Trap Generation and Transient Trap Occupancy Model for Time Evolution of NBTI During DC Multi-Cycle and AC Stress
N. Goel, T. Naphade and S. Mahapatra, Indian Institute of Technology Bombay
3:35 p.m.

4A.4 Self-Heating and its Implications on Hot Carrier Reliability Evaluations (Invited)
S. Mittl and F. Guarín, IBM Corporation

4A.5 Separation of Interface States and Electron Trapping for Hot Carrier Degradation in Ultra-Scaled Replacement Metal Gate n-FinFETs
M. Wang, Z. Liu, T. Yamashita, J. Stathis and C.-y. Chen*, IBM @ Albany Nanotech, *IBM Research Division, T.J. Watson Research Center*

Session 4B - Soft Error

4B.1 Radiation-Induced Soft Error Rate Analyses for 14 nm FinFET SRAM Devices
S. Lee, I. Kim, S. Ha, C.-s. Yu, J. Noh, S. Pae and J. Park, Samsung Electronics

4B.2 SOI FinFET Soft Error Upset Susceptibility and Analysis
P. Oldiges, K. Rodbell, M. Gordon, J.G. Massey, K. Stawiasz, C. Murray, H. Tang, K. Kim and P. Muller, IBM Corporation

4B.3 Multi-Cell Soft Errors at the 16-nm FinFET Technology Node
N. Tam, B. Bhuva, L. Massengill*, D. Ball*, M. McCurdy*, M. Alles* and I. Chaterjee**, Marvell Semiconductor, *Vanderbilt University, **University of Bristol*

4B.4 Terrestrial SER Characterization for Nanoscale Technologies: A Comparative Study
N. Mahatme^^^, B. Bhuva, N. Gaspard, T. Assis, Y. Xu*, P. Marcoux**, M. Vilchis**, B. Narasimham***, A. Shih^, S.-J. Wen^, R. Wong^, N. Tam^^, M. Shroff^^^, S. Koyama[#] and A. Oates[##], Vanderbilt University, *Altera Corporation, **Avago Technologies, ***Broadcom, ^Cisco Systems, Inc., ^^Marvell Technology, ^^^Freescale Semiconductor, Inc., [#]Renesas Electronics, [##]TSMC*

Session 4C - 3D/TSV

4C.1 Impact of 3D Copper TSV Integration on 32SOI FEOL and BEOL Reliablity (Invited)
M. Farooq, G. Larosa, F. Chen, P. Periasamy, T. Graves-Abe, C. Kothandaraman, C. Collins, W. Landers, J. Oakley, J. Liu, J. Safran, S. Ghosh, S. Mittl, D. Ioannou, C. Graas, D. Berger and S. Iyer, IBM Corporation

4C.2 Impacts of 3-D Integration Processes on Device Reliabilities in Thinned DRAM Chip for 3-D DRAM (Invited)
K. Lee, J. Bea, M. Murugesan, T. Fukushima, T. Tanaka and M. Koyanagi, Tohoku University

4C.3 A Highly Reliable DRAM 3-D Wafer Thinning Process
A. Ditali, B. Black, M. Ma, M. Ball, G. Wei and J.M. Brand, Micron Technology, Inc.
3:35 p.m.

4C.4 Device Performance Analysis on 20nm Technology Thin Wafers in a 3D Package
S. Kannan, R. Agarwal, A. Bousquet, G. Aluri and H.-S. Chang, GLOBALFOUNDRIES Inc.

4C.5 Impact of Oxide Liner Properties on TSV Cu Pumping and TSV Stress (Invited)
J. De Messemaeker, O. Varela Pedreira, A. Moussa, N. Nabiollahi, K. Vanstreels, S. Van Huylenbroeck, H. Philipsen, P. Verdonck, B. Vandevelde, I. De Wolf, E. Beyne and K. Croes, imec

POSTER PRESENTATIONS
3D/TSV

3D-1 TSV/FET Proximity Study Using Dense Addressable Transistor Arrays
R. Robertazzi, K. Agarwal, B. Webb and C. Tyberg, IBM

BEOL Dielectrics

BD-1 Electrical and Reliability Performance of Atomic Layer Deposition HfO_2 Capping Layer on Porous Low Dielectric Constant Materials
K.-C. Kao, C.-J. Huang, C.-S. Wu and Y.-L. Cheng, National Chi-Nan University

BD-2 The Reversed Intrinsic Curve and Voltage Dependence for Ultra-low k Dielectric
W. K. Chien, A. Y. Zhao, L. Zhang and F. Cheng, Semiconductor Manufacturing International Corp.

BD-3 Effects of Copper CMP and Post Clean Process on VRDB and TDDB at 28nm and Advanced Technology Node
L. C. Hsu, Y. M. Lin, C. L. Wu, W. K. Lee, Y.-C. Liu, C.-P. Chiu, H. K. Hsu, C-Y Wang, C-C Huang and C. F. Lin, United Microelectronics Corporation

BD-4 A Moisture-Related down Mechanism in Low-k Dielectrics using a Multiple I-V Ramp Test
S. Ogden, J. Borja, H. Zhou, J. Plawsky, T.-M. Lu and W. Gill, Rensselaer Polytechnic Institute

BD-5 Impact of Process Variability on BEOL TDDB Lifetime Model Assessment
K. Croes, D. Kocaay, I. Ciofi, J. Bömmels and Z. Tőkei, Imec

BD-6 Thickness Dependence on Electrical and Reliability Properties for Dense and Porous Low Dielectric Constant Materials
K.-C. Kao, C.-J. Huang, C.-S. Wu and Y.-L. Cheng, National Chi-Nan University

Circuits Aging/Circuit Reliability

CA-1 NBTI and HCD Aware Behavioral Models for Reliability Analysis of Analog CMOS Circuits
N. Heidmann, N. Hellwege, S. Paul and D. Peters-Drolshagen, University of Bremen

CA-2 Negative Bias Temperature Instability Caused by Plasma Induced Damage in 65 nm Bulk and Silicon On Thin BOX (SOTB) Processes
R. Kishida, A. Oshima and K. Kobayashi, Kyoto Institute of Technology

CA-3 A fWLR Test Structure and Method for Device Reliability Monitoring using Product Relevant Circuits
R. Vollertsen, G. Georgakos, K. Kölpin and C. Olk, Infineon Technologies AG

CA-4 Impact of Gate Oxide down in Logic Gates from 28nm FDSOI CMOS Technology
M. Saliva, F. Cacho, C. Ndiaye, V. Huard, D. Angot, A. Bravaix and L. Anghel**, STMicroelectronics, *IM2NP-ISEN, **TIMA*

CA-5 Impact of Time-Zero and NBTI Variability on Sub-20nm FinFET Based SRAM at Low Voltages
N. Goel, P. Dubey, J. Kawa** and S. Mahapatra, IIT Bombay, *Synopsys India Pvt. Ltd., **Synopsys, Inc.*

CA-6 Workload-dependent BTI Analysis in a Processor Core at High Level
O. Heron, C. Sandionigi, E. Piriou, S. Mbarek, V. Huard, CEA LIST, *STMicroelectronics*

CA-7 Duty Cycle Shift Under Static/Dynamic Aging in 28nm HK-MG Technology
K. Sutaria, P. Ren, A. Mohanty, X. Feng*, R. Wang, R. Huang* and Y. Cao, Arizona State University, *Peking University*

Compound/Optoelectronics

CD-1 Degradation Rate for Surface Pitting in GaN HEMT
B. Paine, V. Ng, S. Polmanter, N. Kubota and C. Ignacio, Boeing Network and Space Systems

CD-2 High-Voltage Stress Time-Dependent Dispersion Effects in AlGaN/GaN HEMTs
M. Wespel, M. Dammann, V. Polyakov, R. Reiner, P. Waltereit, B. Weiss, R. Quay, M. Mikulla and O. Ambacher, Fraunhofer Institute for Applied Solid State Physics

CD-4 Threading Dislocations in III-V Semiconductors: Analysis of Electrical Conduction
V. Iglesias, M. Porti, C. Couso, Q. Wu, S. Claramunt, M. Nafría, E. Miranda, N. Domingo**, G. Bersuker** and A. Cordes**, Universitat Autònoma de Barcelona, *ICN2, **Sematech*

Chip Packaging Reliability

CP-1 Mechanical Reliability Assessment of 28nm Back End of Line (BEoL) Stack using Finite Element Analysis and Validation
K. Vishwanath Machani, H. Geisler, D. Breuer, F. Kuechenmeister and J. Paul, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG

CP-3 Contact Resistance of Solder Bump with Low Cost Photosenstive Polyimide for High Performance SoC
J. Park, J. Hong, M. Lee, D. Sun, K. Kang, T. Kim, S. Kim, S. Kown, C. Joo, S. Ha, W. Kim, J. Ryu and S. Pae, Samsung Electronics

CP-4 Reliability of Fine Pitch COF: Influence of Surface Morphology and CuSn Intermetallic Compound Formation
J. Park, M. Lee, K. Min, J.-K. Choi, C.-K. Joo, S.-C. Park, H. Kang and S. Pae, Samsung Electronics Co., Ltd.

CP-5 High Voltage Robustness of Mold Compounds under Different Environmental Conditions
J. Paye, A. Claudi and M. Stecher, Infineon Technologies AG, *University Kassel*

CP-6 Coupled Accelerated Stress Tests for Comprehensive Field Reliability – Synergistic Effects of Moisture and Temperature Cycling
A. Aggarwal, K. Enamul, D. Huitink, N. Sinha, E. Armagan, K. Cao, Intel Corporation

ESD/Latch-up

EL-2 ESD Protection of High Trigger Current 20V HV-SCR with Low Trigger Voltage
K. Cho, J. Kim, K. Noguchi, J. Jang, U. Kwon, K.-H. Lee and Y. Park, Samsung Electronics Co. Ltd.

EL-3 ESD Protection Clamp with Active Feedback and Mis-Trigger Immunity in 28nm CMOS Process
S. Parthasarathy, J. Salcedo, S. Herrera, J.-J. Hajjar, Analog Devices, Inc

EL-4 A Novel High Level ESD FDNSCR with Drain Side Engineering in PMIC Application
Y.-N. He, J.-M. Wang, T.-H. Tang and K.-C. Su, United Microelectronics Corp.

EL-5 Robust ESD Self-Protected LDNMOSFET by an Enhanced Displacement-Current Triggering
*T.-C. Kao, C.-H. Lien, C.-W. Chiu**, J.-H. Lee*, Y.-H. Lo, C.-Y. Hung, T.-Y. Huang** and H.-D. Su**, National Tsing Hua University, *GlobalFoundries Inc., **Richtek Technology Corporation*

EL-6 Enhanced CDM-Robustness for the Packaged IC with the Extra Bonding Wire to the Die-Attach Plate
T.-C. Kao, J.-H. Lee, C.-H. Lien, C.-H. Wang**, K.-C. Tai** and H.-D. Su*, National Tsing Hua University, *GlobalFoundries, Inc, Richtek Technology Corporation*

Electronic Systems Reliability

ER-1 Understanding the Underlying Degradation Physics for Proper Time-To-Failure Distribution Selection
J.W. McPherson, McPherson Reliability Consulting

Failure Analysis

FA-1 Electrical Model of an NMOS Body Biased Structure in Triple-well Technology Under Photoelectric Laser Stimulation
N. Borrel, C. Champeix, M. Lisart, A. Sarafianos, E. Kussener, W. Rahajandraibe* and J.-M. Dutertre**, STMicroelectronics, *Aix Marseille Université IM2NP, **Ecole Nationale Supérieure des Mines de St-Etienne*

FA-2 Mechanical and Thermal Stresses Characterization Maps on Cross-sections of Forward Biased Electronic Power Devices
T. Kociniewski and Z. Khatir, University of Versailles St Quentin and * SATIE (IFSTTAR)*

FA-3 Short Localization in CPU FlipChip using Thermal Imaging and Magnetic Current Imaging
J. Gaudestad, A. Orozco and J. Chen, Neocera, LLC, *Honyang Global Technology Co., LTD.*

FA-4 Employing Transistor Reliability Testing as an FA Tool for Understanding HTOL Product BIST Failures
A. Yassine, L. Blair and W. Seifert, Advanced Micro Devices, Inc.

Gate Dielectrics Reliability

GD-1 The Impacts of Inverter-like Transitions on Device TDDB and Ring Oscillators
T.-Y. Yew, Y.-C. Huang, M.-H. Hsieh, W. Wang, R. Hsieh, Y.-H. Lee and K. Wu, Taiwan Semiconductor Manufacturing Company

GD-3 Extended TDDB Power-law Validation for High-Voltage Applications Such as OTP Memories in High-k CMOS 28nm FDSOI Technology
*A. Benoist, S. Denorme, X. Federspiel, B. Allard and P. Candelier, Université de Lyon, *STMicroelectronics*

Interconnect Metallization Reliability

IT-1 Exploration of Electromigration and Joule Heating Effect Associated with Un-silicided N+ Poly
X.-F. Zhao, A. Zhao, V. Chang, J. Wu, M. Li, M. Zhang and W.-T. Kary Chien, Semiconductor Manufacturing International Corp.

IT-2 Interconnect Design Study for Electromigration Reliability Improvement
*G. Marti, L. Arnaud**, D. Ney and Y. Wouters*, STMicroelectronics, *SIMaP, **CEA-Leti Minatec*

IT-3 Wafer-level Electromigration for Reliability Monitoring: Quick-turn Electromigration Stress with Correlation to Package-level Stress
D. Slottke, R.J. Kamaladasa, M. Harmes, I. Tsameret, M. Kobrinsky, T. McMullen and J. Dunklee**, Intel Corporation, *Cascade Microtech Inc., **Celadon Systems Inc.*

Memory

MY-1 Analysis of SET and RESET States Drift of Phase-Change Memories by Low Frequency Noise Measurements
S. Souiki-Figuigui, V. Sousa, G. Ghibaudo, G. Navarro, M. Coue, L. Perniola, P. Zuliani** and R. Annunziata**, CEA/LETI, *IMEP-LAHC, **STMicroelectronics*

MY-2 A Collective Relaxation Model for Resistance Drift in Phase Change Memory Cells
A. Sebastian, D. Krebs, M. Le Gallo, H. Pozidis and E. Eleftheriou, IBM Research - Zurich

MY-3 Investigation of the Data Retention Mechanism and Modeling for the High Reliability Embedded Split-Gate MONOS Flash Memory
Y. Kawashima, T. Hashimoto and I. Yamakawa, Renesas Electronics Corporation, *Hitachi, Ltd.*

MY-4 Data Retention Statistics and Modelling in HfO_2 Resistive Switching Memories
S. Ambrogio, S. Balatti, Z.-Q. Wang, Y.-S. Chen, H.-Y. Lee*, F.T. Chen and D. Ielmini, Politecnico di Milano, *Industrial Technology Research Institute (ITRI)*

MY-5 RTS Noise Reduction of 1Y-nm Floating Gate NAND Flash Memory Using Process Optimization
S. Kim, M. Lee, G.-B. Choi, J. Lee, Y. Lee, M. Cho, K.-O. Ahn and J. Kim, SK Hynix Inc.

MY-6 Cycling Pattern and Read/Bake Conditions Dependence of Random Telegraph Noise in Decananometer NAND Flash Arrays
C. Miccoli, G.M. Paolucci, C. Monzio Compagnoni*, A.S. Spinelli* and A. Goda, Micron Technology Inc., *Politecnico di Milano*

MY-7 Conductive Filaments Multiplicity as a Variability Factor in CBRAM
U. Celano, L. Goux, A. Belmonte, K. Opsomer, C. Detavernier, M. Jurczak and W. Vandervorst, imec, *University of Gent*

MY-8 Improvement of Oxide Reliability in NAND Flash Memories Using Tight Endurance Cycling with Shorter Idling Period
R. Shirota, B.-J. Yang, Y.-Y. Chiu, Y.-T. Wu, P.-Y. Wang, J.-H. Chang*, M. Yano*, M. Aoki*, T. Takeshita*, C.-Y. Wang* and I. Kurachi**, National Chiao-Tung University, *Winbond Electronics Corporation, **High Energy Accelerator Research Organization*

MY-9 SRAM Stability Design Comprehending 14nm FinFET Reliability
C. Bae, S. Pae, C.-s. Yu, K. Kim, Y. Kim and J. Park, Samsung Electronics

MY-11 Oxygen Vacancy Traps in Hi-K/Metal Gate Technologies and Their Potential for Embedded Memory Applications
C. Kothandaraman, X. Chen, D. Moy, D. Lea, S. Rosenblatt, F. Khan, D. Leu, T. Kirihata, D. Ioannou, G. LaRosa, J. Johnson, N. Robson and S. Iyer, IBM Microelectronics

MY-12 Impact of Nanoscale Polarization Relaxation on Endurance Reliability of One-Transistor Hybrid Memory Using Combined Storage Mechanisms
Y.-C. Chiu, C.-Y. Chang, H.-H. Hsu C.-H. Cheng and M.-H. Lee*, National Chiao-Tung University, National Taiwan Normal University*

MY-13 Four Point Probe Ramped Voltage Stress as an Efficient Method to Understand down of STT-MRAM MgO Tunnel Junctions
S. Van Beek, K. Martens*, P. Roussel, G. Donadio, J. Swerts, S. Mertens, G. Kar, T. Min and G. Groeseneken*, Imec, *KU Leuven*

Process Integration

PI-1 An Investigation of Process Dependence of Porous IMD TDDB
W.Y. Zhang, M.C. Silvestre, A. Selvam, E. Ramanathan, C. Ordonio, J. Schaller, T. Shen, K.B. Yeap, C. Capasso, P. Justison and J.H. Lee, GLOBALFOUNDRIES Inc.

PI-2 New Insight in Plasma Charging Impact on Gate Oxide down in FDSOI Technology
M. Akbal, G. Ribes and L. Vallier, STMicroelectronics, *LTM/CNRS*

PI-3 Reliability of $HfAlO_x$ in Multi Layered Gate Stack
M.N. Bhuyian and D. Misra, New Jersey Institute of Technology

Product IC Reliability

PR-1 A Failure Physics Model for Hardware Trojan Detection Based on Frequency Spectrum Analysis
C. He, B. Hou, L. Wang, Y. En and S. Xie, No.5 Electronics Research Institute of the Ministry of Industry and Information Technology

PR-2 Printed Circuit Board (PCB) Charge Induced Prodcut Yield-Loss During the Final Test
J.-H. Lee, K. Takahashi, M. Prabhu and M.I. Natarajan, GLOBALFOUNDRIESInc.

Soft Error

SE-1 Investigation of Single Event Upset and Total Ionizing Dose in FeRAM for Medical Electronic Tag
T. Uemura and M. Hashimoto, Osaka University

SE-2 Soft Error Immunne Latch Design for 20 nm Bulk CMOS
T. Uemura, T. Kato, H. Matsuyama and M. Hashimoto, Fujitsu Semiconductor, *Osaka University*

SE-3 Techniques for Heavy Ion Microbeam Analysis of FPGA SER Sensitivity
A. Evans, D. Alexandrescu, V. Ferlet-Cavrois and K.-V. Obbe**, IROC Technologies, *ESA/ESTEC, **GSI*

SE-4 Analysis of Advanced Circuits for SET Measurement
R. Liu, A. Evans, Q. Wu, Y. Li, L. Chen, S.-J. Wen**, R. Wong** and R. Fung**, University of Saskatchewan, *IROC Technologies, **Cisco Systems*

SE-6 Impact of Package on Neutron Induced Single Event Upset in 20 nm SRAM
T. Uemura, T. Kato, H. Matsuyama and M. Hashimoto, Fujitsu Semiconductor, *Osaka University*

SE-7 Alpha Soft Error Rate of FDSOI 28 nm SRAMs: Experimental Testing and Simulation Analysis
V. Malherbe, G. Gasiot, D. Soussan, A. Patris, J.-L. Autran* and P. Roche, STMicroelectronics, *Aix-Marseille University & CNRS, IM2NP*

SE-9 Frequency and Voltage Effects on SER on a 65nm Sparc-V8 Microprocessor Under Radiation Test
C. Bottoni, B. Coeffic, J.-M. Daveau, G. Gasiot, F. Abouzeid, S. Clerc, L. Naviner and P. Roche, STMicroelectronics, *Telecom ParisTech*

SE-11 MBU-Calc: A Compact Model for Multi-Bit Upset (MBU) SER Estimation
W. Wu and N. Seifert, Intel Labs

SE-12 Logic Soft Error Study with 800-MHz DDR3 SDRAMs in 3x nm Using Proton and Neutron Beams
G.Y. Bak, S. Lee, H. Lee, K. Park, S. Baeg, S.J. Wen, R. Wong* and C. Slayman*, Hanyang University, *Cisco Systems Inc.*

Transistors

XT-1 New LFN and RTN Analysis Methodology in 28 and 14nm FD-SOI MOSFETs
C. Theodorou, E. Ioannidis, S. Haendler, N. Planes*, E. Josse*, C. Dimitriadis** and G. Ghibaudo, IMEP-LAHC, MINATEC, *STMicroelectronics, **Aristotle University of Thessaloniki*

XT-2 Hot-Carrier Degradation in Single-Layer Double-Gated Graphene Field-Effect Transistors
Y. Illarionov, M. Waltl, A. Smith, S. Vaziri*, M. Ostling*, T. Mueller, M. Lemme** and T. Grasser, TU Wien, *KTH Royal Institute, **University of Siegen*

XT-4 Impact of DC and RF Non-Conducting Stress on nMOS Reliability
A. Cattaneo, S. Pinarello, J.-E. Mueller and R. Weigel, Intel Mobile Communications, *University of Erlangen-Nuremberg*

XT-5 Investigation of Nitrogen Enhanced NBTI Effect Using the Universal Prediction Model
P. Wu, C. Ma**, L. Zhang, X. Lin* and M. Chan, The Hong Kong University of Science and Technology, * Peking University*

XT-6 Comprehensive Understanding of Hot Carrier Degradation in Multiple-fin SOI FinFETs
*H. Jiang, L. Yin, Y. Li, N. Xu**, K. Zhao*, Y. He, G. Du, X. Liu and X. Zhang, Peking University, *Beijing Information Science and Technology University, **University of California at Berkeley*

XT-7 PBTI and HCI Degradations of Ultrathin Body InGaAs-on-Insulator nMOSFETs Fabricated by Wafer Bonding
X. Tang, J. Lu, R. Zhang, Y. Zhao, W. Wu, C. Liu*, Y. Shi*, Z. Huang** and Y. Kong**, Zhejiang University, *Nanjing University, **Nanjing Electronic Devices Institute*

Session 5A - Gate Dielectrics Reliability

5A.1 General Features of Progressive down in Gate Oxides: A Compact Model (Invited)
F. Palumbo, M. Eizenberg and S. Lombardo, Technion, *CNR-IMM*

5A.2 Spectroscopy of SILC Trap Locations and Spatial Correlation Study of Percolation Path in the High-K and Interfacial Layer
N. Raghavan, M. Bosman and K.L. Pey, Singapore University of Technology and Design (SUTD), *A*STAR*

5A.3 On the Volatility of Oxide Defects: Activation, Deactivation, and Transformation
T. Grasser, M. Waltl, W. Goes, Y. Wimmer, A.-M. El-Sayed, A.L. Shluger* and B. Kaczer**, TU Wien, *UCL, **imec*

5A.5 Physical Understanding of Low Frequency Degradation of NMOS TDDB In High-K Metal Gate Stack-Based Technology. Implication on Lifetime Assessment
A. Bezza, M. Rafik, D. Roy, X. Federspiel, P. Mora, C. Diouf, V. Huard and G. Ghibaudo, STMicroelectronics, *IMEP-LAHC*

5A.6 A New TDDB Lifetime Model for AC Inverter-like Stress in Advance FinFET Structure
I.K. Chen, C.L. Chen, Y.-H. Lee, R. Lu, Y.W. Lee, H.H. Hsu, Y.W. Tseng, Y.W. Lin and J.R. Shih, TSMC.

5A.7 The Relationship Between Border Traps Characterized By AC Admittance and BTI in III-V MOS Devices
A. Vais, K. Martens, J. Franco, D. Lin, A. Alian, P. Roussel, S. Sioncke, N. Collaert, A. Thean, M. Heyns, G. Groeseneken and K. DeMeyer, imec

Session 5B – Memory

5B.1 Scaling and Write Error Rate of Perpendicular Spin Torque MRAM (Invited)
D. Worledge, IBM Research

5B.3 Understanding Pulsed-cycling Variability and Endurance in HfO_x RRAM
S. Balatti, S. Ambrogio, Z. Wang, S. Sills, A. Calderoni*, N. Ramaswamy* and D. Ielmini, Politecnico di Milano and IU.NET, *Micron Technology Inc.*

5B.4 A New Prediction Method for ReRAM Data Retention Statistics Based on 3D Filament Structures
Z. Wei, K. Katayama, S. Muraoka, R. Yasuhara, T. Mikawa and K. Eriguchi, Panasonic Corporation, *Kyoto University*

5B.5 A Microscopic Physical Description of RTN Current Fluctuations in HfO_x RRAM
F.M. Puglisi, P. Pavan, L. Vandelli, A. Padovani, M. Bertocchi and L. Larcher, Università di Modena e Reggio Emilia

5B.2 Monte Carlo Model of Reset Stochastics and Failure Rate Estimation of Read Disturb Mechanism in HfO_x RRAM
N. Raghavan, D. Frey, M. Bosman** and K.L. Pey, Singapore University of Technology and Design (SUTD), *Massachusetts Institute of Technology (MIT), **A*STAR Institute of Materials Research and Engineering (IMRE)*

5B.6 Phase-Change Memory: Feasibility of Reliable Multilevel-cell Storage and Retention at Elevated Temperatures
M. Stanisavljevic, A. Athmanathan, N. Papandreou, H. Pozidis and E. Eleftheriou, IBM Research – Zurich

5B.7 Impact of P/E Cycling on Read Current Fluctuation of NOR Flash Memory Cell: A Microscopic Perspective Based on Low Frequency Noise Analysis
X. Yang, J. Liu, Z. Zheng, Y. Wang, D. Jiang, S. Chiu, H. Wu* and M. Liu, Chinese Academy of Sciences, *Semiconductor Manufacturing International Corporation (SMIC)*

Session 5C - Chip Packaging Reliability

5C.1 Probabilistic Design for Reliability in Electronics and Photonics: Role, Significance, Attributes, Challenges (Invited)
E. Suhir, A. Bensoussan, G. Khatibi** and J. Nicolics**, Portland State University, *Institute of Technological Research (IRT), **Technical University*

5C.2 The Electromigration Behavior of Copper Pillars for Different Current Directions and Pillar Shapes
C. Hau-Riege, Y.W. Yau, K. Caffey, R. Kumar, Y.Y. Sun, A. Bao, M. Shah, L. Zhao, O. Bchir, A. Syed and S. Bezuk, Qualcomm Inc.

5C.3 Scenario for Catastrophic Failure in Interconnect Structure under Chip Package Interaction
M. Omiya, S. Kamiya, N. Shishido*, K. Koiwa*, H. Sato*, M. Nishida*, T. Suzuki**, T. Nakamura**, T. Suzuki*** and T. Nokuo***, Keio Universtiy, *Nagoya Institute of Technology, **Fujitsu Laboratories Ltd., ***JEOL, Ltd.*

5C.4 Semi-Empirical Stress-based Acceleration of Temperature Cycling Failure
D. Huitink and A. Lucero, Intel Corporation

5C.5 CPI Reliability and EMI Benefit for MIM CAP Embedded C4 Package
H. Chun, I.H. Baick, S.-S. Ha, E. Kwon, S. Lee, S. Kim, S. Pae and J. Park, Samsung Electronics

5C.6 Package Induced Stress Impact on Transistor Performance for Ultra-thin SoC
M. Kabir, D. Young, B. Kilic, I. Sauciuc, C. Sapp and G. Leatherman, Intel Corporation

Session 6A - Circuit Aging/Circuit Reliability

6A.1 Non-volatile Memory as Hardware Synapse in Neuromorphic Computing: A First Look at Reliability Issues

(Invited)
R. Shelby, G. Burr, I. Boybat and C. di Nolfo, IBM Almaden Research Center
.

6A.2 Long-term Data for BTI Degradation in 32nm IBM Microprocessor using HKMG Technology
P.-F. Lu, K. Jenkins, K. Paul Muller and R. Schaufler*, IBM Research, Thomas J. Watson Center, *IBM System and Technology Group*

6A.3 A Revolving Reference Odometer Circuit for BTI-Induced Frequency Fluctuation Measurements under Fast DVFS Transients
S. Satapathy, W.H. Choi, X. Wang and C.H. Kim, University of Minnesota, *Intel Corporation*

6A.4 The Impact and Implication of BTI/HCI Decoupling on Ring Oscillator
M.-H. Hsieh, Y.-C. Huang, T.-Y. Yew, W. Wang and Y.-H. Lee, Taiwan Semiconductor Manufacturing Company

6A.5 Assessing Intrinsic and Extrinsic End-of-Life Risk Using Functional SRAM Wafer Level Testing
Y.M. Randriamihaja, W. McMahon, S. Balasubramanian, T. Nigam, B. Parameshwaran, R. Mann, T. Klick, T. Schaefer, A. Kumar, Y. Song, V. Joshi, R. Ranjan and F. Chen, GLOBALFOUNDRIES, *Purdue University*
.

6A.6 SRAM Vmax Stability Considerations
D. Burnett, S. Balasubramanian, V. Joshi, S. Parihar, J. Higman and C. Weintraub, GLOBALFOUNDRIES Inc
.

Session 6B - Product IC Reliability

6B.1 28nm UTBB FDSOI Product Reliability/ Performance Trade-off Optimization Through Body bias Operation
P. Mora, X. Federspiel, F. Cacho, V. Huard and W. Arfaoui, STMicroelectronics

6B.2 Product-Level Reliability Estimator with Budget-Based Reliability Management in 20nm Technology
J.-G. Ahn, M.F. Lu, N. Navale, D. Graves, P.-C. Yeh, J. Chang and S.Y. Pai, Xilinx, Inc.

6B.3 From BTI Variability to Product Failure Rate: A Technology Scaling Perspective
V. Huard, D. Angot and F. Cacho, STMicroelectronics

6B.4 Analyzing Path Delays for Accelerated Testing of Logic Chips
E. Ray, B. Linder, R. Robertazzi, K. Stawiasz, A. Weger, E. Yashchin, J. Stathis and P. Song, IBM Thomas J. Watson Research Center

6B.5 CpK Approach for the Qualification of ECC-Designs with Single Bit Failures
G. Tempel, Infineon Technologies Dresden GmbH

Session 6C - Compound/Optoelectronics

6C.1 Commercialization and Reliability of 600V GaN Power Switches (Invited)
T. Kikkawa, T. Hosoda, K. Shono, K. Imanishi, Y. Asai, Y. Wu, L. Shen*, K. Smith*, D. Dunn*, S. Chowdhury*, P. Smith*, J. Gritters*, L. McCarthy*, R. Barr*, R. Lal*, U. Mishra* and P. Parikh, Transphorm Japan, Inc. *Trrransphorm, Inc.*

6C.2 Thermal Activation of PBTI-related Stress and Recovery Processes in GaN MIS-HEMTs using on-wafer Heaters
P. Lagger, S. Donsa, P. Spreitzer, G. Pobegen, M. Reiner, H. Naharashi, J. Mohamed, H. Mösslacher, G. Prechtl, D. Pogany** and C. Ostermaier, Infineon Technologies Austria AG, *Kompetenzzentrum für Automobil- und Industrieelektronik, **Vienna University of Technology*

6C.3 Origin of Physical Degradation in AlGaN/GaN on Si High Electron Mobility Transistors under Reverse bias Stressing
W.A. Sasangka, G.J. Syaranamual, C.L. Gan and C.V. Thompson, Singapore-MIT Alliance for Research and Technology

6C.4 Time Dependent Dielectric down (TDDB) Evaluation of PE-ALD SiN Gate Dielectrics on AlGaN/GaN Recessed Gate D-mode MIS-HEMTs and E-mode MIS-FETs
T.-L. Wu, D. Marcon, B. De Jaeger, M. Van Hove, B. Bakeroot, S. Stoffels, G. Groeseneken, S. Decoutere and R. Roelofs, imec, *ASM*

6C.5 Positive-Bias Temperature Instability (PBTI) of GaN MOSFETs

A. Guo and J. del Alamo, Massachusetts Institute of Technology

6C.6 Instabilities of SiC MOSFETs During use Conditions and Following bias Temperature Stress
G. Pobegen and A. Krassnig, Kompetenssentrum für Automobil- und Industrieelektronik (KAI) BmbH