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ER.3 Models and Methods for Determining Storage Reliability, A. Mense, L. Gullo, J. Thomas, P. Shedlock, Raytheon Missle Systems

FA.1 Failure Recovery Mechanism Caused by Secondary Defect, S. Karki, D. Nguyen, Texas Instruments

GD.1 New Insight on High-k/Metal Gate Reliability Modeling for Providing Guidelines for Process Development, M. Rafik, G. Ribes, P. Mora, S. Blonkowski, X. Federspiel, P. Caubet,C. Gaumer, M. Grosjean, D. Roy, STMicroelectronics

GD.2 On the Meaning of Charge Pumping Curve Edges, D. Bauza, IMEP-LAHC Minatec INPGrenoble

GD.3 Reliability in Gate First and Gate Last Ultra-Thin-EOT Gate Stacks Assessed with CV-eMSM BTI Characterization, E.Bury, B. Kaczer, H. Arimura, M. Toledano Luque, L. Å. Ragnarsson, P. Roussel, A. Veloso, S.A. Chew, M. Togo, T. Schram, G. Groeseneken, KU Leuven, IMEC

GD.5 Demonstrating Distribution of SILC Values at Individual Leakage Spots, T. Inatsuka, R. Kuroda, A. Teramoto, Y. Kumagai, S. Sugawa, T. Ohmi, Tohoku University

ME.1 Estimating the Detection Stability of a Si Nanowire Sensor Using an Additional Charging Electrode, M.-C. Chen, H.-C. Chen*, T.-H. Lee*, Y.-H. Lin**, J.-H. Shih**, B.-W. Wang^, Y.-F. Hou, Y.-J. Chen, C.-Y. Lin, C.-H. Lin, Y-P Hsieh#, C. Ho, M.-Y. Hua*, J.-T. Qiu*, T. Wang^, F.-L. Yang, National Nano Device Laboratories, *Chang Gung University, **National United University, ^National Chiao-Tung Univ., #National Cheng Kung Univ.y

ME.2 Morphological Analysis of GaN Membranes Obtained by Micromachining of GaN/Si, A. Cismaru, A. Muller, F. Comanescu, M. Purica, A. Stefanescu, A. Dinescu, G. Konstantinidis*, A. Stavrinidis*, IMT – Bucharest, *FORTH – Heraklion

ME.3 Spectroscopic Analysis of Material Transfer Phenomena in MEMS Switches, A. Peschot, C. Poulain, H. Sibuet, F. Souchon, N. Bonifaci*, O. Lesaint*, CEA, LETI, *G2Elab

MY.1 The Effect of Hydrogen on Program Disturbance in Sub-2ynm Nand Flash, Y. Jaewook, W. Cha, S. Seo, H. Oh, J. Oh, H. Shim, S. Choi, B-K. Kim, S. Cho, K. Kim, K-O Ahn and G. Bae, SK Hynix Inc. Inc.

MY.2 Stastical Assessment of Endurance Degradation in High and Low Resistive States of the HfO_2-Based RRAM, S. Deora, G. Bersuker, M.G. Sung, D.C. Gilmer and P.D. Kirsch, H-F Li*, H. Chong* and S. Gausepohl*, SEMATECH and *CNSE

MY.3 The Physical Insights into an Abnormal Erratic Behavior in the Resistance Random Access Memory, Y.J. Huang, S.S. Chung, H.Y. Lee, Y.S. Chen, F.T. Chen, P.Y. Gu, M.J. Tsai, National Chiao Tung University, ITRI

MY.4 Program/Erase Speed, Endurance, Retention, and Disturbance Characteristics of Single-Poly Embedded Flash Cells, S.-H. Song, J. Kim, C.H. Kim, University of Minnesota

MY.5 Reliable, Low-Power Super-Lattice Phase-Change Memory without Melting and Write-Pulse Down Slope, K. Johguchi, T. Egami, K. Takeuchi, Chuo University

MY.6 Instability Study of high-k IPD Stacks on Hybrid Floating Gate Flash Memory, M.B. Zahid, R. Degraeve, L. Breuil, G. Van Den Bosch, J. Van Houdt, IMEC

MY.7 Investigation of Data Retention Window Closure on Logic Embedded Non-volatile Memory, Y.-Y. Liao, L.Y. Tsai, Y. Leu, Y-H Lee, W. Wang and K. Wu, TSMC

MY.8 Reliability Study of Carbon-Doped GST Stack Robust Against Pb-Free Soldering Reflow, S. Souiki, Q. Hubert, G. Navarro, A. Persico, C. Jahan, E. Henaff, V. Delaye, D. Blachier, V. Sousa, L. Perniola, E. Vianello, B. De Salvo, CEA-LETI and IMEP-LAHC

MY.9 Electrical Performances of SiO2-doped GeTe for Phase-Change Memory Applications, G. Navarro, A. Persico, E. Henaff, F. Aussenac, P. Noé, C. Jahan, L. Perniola, V. Sousa, E. Vianello, B. De Salvo, CEA - LETI, MINATEC Campus

MY.10 Random Telegraph Noise (RTN) in Scaled RRAM Devices, D. Veksler, G. Bersuker, L. Vandelli*, A. Padovani*, L. Larcher*, A. Muraviev, B. Chakrabarti**, E. Vogel**, D. Gilmer, P.D. Kirsch, SEMATECH, *Università degli studi di Modena e Reggio Emilia, **UT Dallas, Georgia Institute of Technology

MY.11 180nm FRAM Reliability Demonstration with 10 Years Data Retention at 125°C, J. Rodriguez, J. Rodriguez-Latorre, C. Zhou, A. Venugopal, A. Acosta, M. Ball, P. Ndai, S. Madan, H. McAdams, K.R. Udayakumar, S. Summerfelt, T. San, T. Moise, Texas Instruments Inc.

MY.12 Drain Stress Influence on Read Disturb Defectivity, M. De Tomasi, R.E. Vaion, L. Cola, P. Zabberoni, A. Mervic, STMicroelectronics

PI.1 New Electrical Testing Structures and Analysis Method for MOL and BEOL Process Diagnostics and TDDB Reliability Assessment, F. Chen, S. Mittl, M. Shinosky, R. Dufresne, J. Aitken, Y. Wang, K. Kolvenback, W. Henson, D. Mocuta, IBM

PI.2 Reliability Studies of a 22nm SoC Platform Technology Featuring 3-D Tri-Gate, Optimized for Ultra Low Power, High Performance and High Density Application, A. Rahman, P. Bai, G. Curello, J. Hicks, C.-H. Jan, M. Jamil, J. Park, K. Phoa, M.S. Rahman, C. Tsai, B. Woolery, J.-Y. Yeh, Intel Corporation

PI.3 Impact of Hydrogen in Capping Layers on BTI Degradation and Recovery in High-κ Replacement Metal Gate Transistors, M. Jin, C. Tian*, G. La Rosa, S. Uppal**, W. Mcmahon**, H. Kothari***, Y. Liu**, E. Cartier, W. Lai, A. Dasgupta, S. Polvino, M. Belyansky, A. Chen**, X. Zhou, A. Madan, Y. Yao, N. Klymko, V. Narayanan, SAMSUNG Electronics, *IBM Microelectronics, **GLOBALFOUNDRIES, **ST Microelectronics

PR.1 Product-Level Reliability Estimator with Advanced CMOS Technology, J.-G. Ahn, M. Feng Lu, P.-C. Yeh, J. Chang, X. Wu, S.Y. Pai, Xilinx

SE.1 Modeling of Radiation-Induced Single Event Transients in SOI FinFETS, L. Artola, G. Hubert, R. Schrimpf*, DESP/ONERA , *Vanderbilt University

SE.2 Neutron-Induced Single-Event-Transient Effects in Ultrathin-Body Fully-Depleted Silicon-on-Insulator MOSFETs, J. Bi, R.A. Reed, R.D. Schrimpf, D.M. Fleetwood, Z. Han*, Vanderbilt University, *Chinese Academy of Sciences

SE.3 Single-Event Transient Measurement on a DC/DC PWM Controller Using Pulsed X-ray, Y. Ren, L. Chen, S. Shi*, G. Guo*, S. Wen***, R. Wong**, N. Van Vonno^, L. Bhuva#, University of Saskatchewan,* China Institute of Atomic Energy,**Canadian Light Source, ***Cisco Systems Inc., ^Intersil Inc., #Vanderbilt University

SE.4 A Comprehensive Soft Error Analysis Tool For Core Networking System, H. Zhu, R. Wong, S. Wen, Cisco

SE.5 Contributions of Charge Sharing and Bipolar Effects to Cause or Suppress MCUs on Redundant Latches, K. Zhang, K. Kobayashi, Kyoto Institute of Technology and JST, CREST

SE.6 Estimation of Hardened Flip-flop Neutron Soft Error Rates using SRAM Multiple-cell Upset Data in Bulk CMOS, N. Gaspard, S. Jagannathan, Z. Diggins, M. McCurdy, T. Loveless, B. Bhuva, L. Massengill, W. Holman, A. Oates*, Y.-P. Fang*, S.-J. Wen**, R. Wong**, K. Lilja***, M. Bounasser***, Vanderbilt University, *TSMC, **Cisco Systems Inc., ***Robust Chip Inc.

SE.7 Effect of Threshold Voltage Implants on Single-event Error Rates of D Flip-flops in 28-nm Bulk CMOS, N. Gaspard, S. Jagannathan, A. Kauppila, T. Loveless, J. Kauppila, B. Bhuva, L. Massengill, W. Holman, A. Oates*, Y.P. Fang*, S.-J. Wen**, R. Wong**, Vanderbilt University, *TSMC, **Cisco Systems Inc.

SE.8 Length and Fin Number Dependence of Ionizing Radiation-Induced Degradation in Bulk FinFETs, I. Chatterjee, E. Zhang, B.Bhuva, D.M. Fleetwood, Y.-P. Fang*, A. Oates*, Vanderbilt University, *TSMC

XT.1 New Hot Carrier Degradation Modeling Reconsidering the Role of EES in Ultra Short N-Channel MOSFETs, Y.M. Randriamihaja, X. Federspiel, V. Huard, A. Bravaix*, P. Palestri**, STMicroelectronic, *ISEN-IM2NP, **DIEGM University of Udine

XT.2 A Comprehensive AC/DC NBTI Model: Stress, Recovery, Frequency, Duty Cycle and Process Dependence, S. Desai, S. Mukhopadhyay, N. Goel, N. Nanaware, B. Jose, K. Joshi, S. Mahapatra, IIT - Bombay

XT.3 Multi-Region DCIV Spectroscopy and Impacts on the Design of STI-based LDMOSFETs, Y. He, G. Zhang, L. Han, X. Zhang, Peking University

XT.4 Recovery Behavior in Negative Bias Temperature Instability, Y. Yonamoto, Hitachi, Ltd.

XT.5 Investigation of Stochastic Implementation of Reaction Diffusion (RD) Model for NBTI Related Interface Traps, T. Naphade, N. Goel, P. Nair, S. Mahapatra, IIT Bombay

XT.6 A Test Structure and Spectroscopic Method for Monitoring Interface Traps, C. Wei, Y. He, G. Zhang, X. Zhang, Peking University

XT.7 The Physical Mechanisms of I_G Random Telegraph Noise in Deeply Scaled pMOSFETs, X. Ji, Y. Liao, C. Zhu, J. Chang, F. Yan, Y. Shi, Q. Guo*, Nanjing University, *Wuhan Xinxin Semiconductor Manufacturing Corp.

XT.8 Effects of Positive and Negative Constant Voltage Stress on Organic TFTs, N. Wrachien, A. Cester, D. Bari, G. Meneghesso, J. Kovac*, J. Jakabovic*, M. Weis*, D. Donoval*, University of Padova, *Slovak University of Technology

XT.9 Interaction Between BTI and HCI Degradation in High-K Devices Application to BTI Deconvolution from HCI in WLR Tests and Product Operation, X. Federspiel, M. Rafik, D. Angot, F. Cacho, D. Roy, STMicroelectronics

XT.10 Detrimental Impact of Hydrogen Passivation on NBTI and HC Degradation, G. Pobegen, M. Nelhiebel, T. Grasser*, KAI GmbH, *TU Vienna

XT.11 The Study of Time Constant Analysis in Random Telegraph Noise at the Subthreshold Voltage Region, A. Yonezawa, A. Teramoto, T. Obara, R. Kuroda, S. Sugawa, T. Ohmi, Tohoku University

SESSION 5A: GATE DIELECTRIC

5A.1 Models of Oxygen Vacancy Defects Involved in Degradation of Gate Dielectrics (Invited), A. Shluger, K. McKenna*, University College London, *The University of York

5A.2 Characterization and Optimization of Charge Trapping in High-K Dielectrics, E. Cartier, T. Ando, M. Hopstaken, V. Narayanan, R. Krishnan*, J.F. Shepard*, M.D. Sullivan*, S. Krishnan*, M.P. Chudzik*, S. De**, R. Pandey**, M. Bajaj**, K. Murali**, A. Kerber***, IBM TJ Watson Research Center, *IBM Microelectronics, **IBM India Semiconductor Research and Development Center, ***GLOBALFOUNDRIES

5A.3 The "Buffering" Role of High-κ in Post Breakdown Degradation Immunity of Advanced Dual Layer Dielectric Gate Stacks, N. Raghavan, A. Padovani*, X. Wu**, K. Shubhakar**, M. Bosman***, L. Larcher*, K.L. Pey**, Nanyang Technological University (NTU), *Università di Modena e Reggio Emilia, **Singapore University of Technology & Design, ***A*STAR

5A.4 A New Formulation of Breakdown Model for High-k/SiO2 Stack Dielectrics, E. Wu, IBM semiconductor Research and Development Center

5A.5 Sub-threshold Current Based Acceleration and Modeling of OFF-state TDDB in Drain Extended NMOS and PMOS Transistors, D. Varghese, A. Venugopal, S. Pan, S. Krishnan, Texas Instruments

5A.6 Compact Analytical Models for the SET and RESET Switching Statistics of RRAM Inspired in the Cell-Based Percolation Model of Gate Dielectric Breakdown, S. Long, X. Lian*, C. Cagli**, L. Perniola**, E. Miranda*, D. Jiménez*, H. Lv, Q. Liu, L. Li, Z. Huo, M. Liu, J. Suñé*, Chiness Academy of Sciences, *Universitat Autònoma de Barcelona,**CEA - LETI

SESSION 5B: FAILURE ANALYSIS

5B.1 Open Localization on Copper Wirebond using Space Domain Reflectometry, J. Gaudestad, V. Talanov, A. Orozco, K.L. Khoo, Neocera LLC, *Altera Malaysia

5B.2 Atomic-Level Study of TDDB Mechanism of Hf-doped SiON Gate Dielectrics using Cs-Corrected STEM and Atom Probe Tomography, S. Kudo, Y. Hirose, K. Funayama, K. Ohgata, M. Inoue, K. Eguchi, A. Nishida, K. Asayama, N. Hattori, T. Koyama, K. Nakamae, Renesas Electronics Corporation

5B.3 ToF-SIMS Characterization of Boron and Phosphorus Distribution in Sub-atmospheric Chemical Vapour Deposition Borophosphosilicate Glass (SA-CVD BPSG) Films, E. Ferlito, G. Pizzo, R. De Gregorio, G. Anastasi, R. Ricciari, D. Mello, STMicroelectronics

5B.4 Localization of Electrical Active Defects caused by Reliability-Related Failure Mechanism by the Application of Lock-in Thermography, C. Schmidt, K. Wadhwa*, A. Reverdy**, E. Reinders***, DCG SystemsGmbH, *DCG Systems, **Sector Technologies, ***MASER Enginerring B.V.

5B.5 Building the Electrical Model of the Pulsed Photoelectric Stimulation of an NMOS Transistor in 90nm Technology, A. Sarafianos, O. Gagliano, V. Serradeil, M. Lisart, J.-M. Dutertre*, A. Tria*, STMicroelectronics, *Centre de Microélectronique de Provence - Georges Charpak

5B.6 Electron Temperature - the Parameter to be Extracted from Backside Spectral Photon Emission (Invited), A. Glowacki, C. Boit, P. Perdu*, Y. Yokoyama**, TUB Berlin University of Technology, *CNES, **Hamamatsu Photonics Deutschland GmbH

SESSION 5C: 3D/CPI

5C.1 Experimental Analyses of the Mechanical Reliability of Advanced BEOL/fBEOL Stacks Regarding CPI Loading (Invited), H. Geisler, E. Schuchardt, M. Brueckner, P. Hofmann, K. Vishwanath Machani, F. Kuechenmeister, D. Breuer, H.-J. Engelmann, GLOBALFOUNDRIES Dresden Module One LLC & Co. KG

5C.2 Delamination in BEOL: Analysis of Interface Failure by Combined Experimental & Modeling Approaches, B. Debecker, K. Vanstreels, M. Gonzalez, B. Vandevelde, IMEC

5C.3 Accelerated Stress Testing Methodology to Risk Assess Silicon-Package Thermo-Mechanical Failure Modes Resulting from Moisture Exposure under use Condition, S. Rangaraj, D. Kwon, M. Pei, J. Hicks, G. Leatherman, A. Lucero, T. Wilson, S. Streit, Jun He, Intel Corporation

5C.4 Reliability Characterization and FEM Modeling of Power Devices under Reptitive Power Pulsing, F. Pozzobon, D. Paci, G. Pizzo, A. Buri, S. Morin, F. Carace, A. Andreini, D. Gastaldi*, E. Bertarelli*, R. Lucchini*, P. Vena*, ST Microelectronics, *Politecnico di Milano

5C.5 Impact of Barrier Integrity on Liner Reliability in 3D Through Silicon Vias, Y. Li, Y. Civale, Y. Oba*, A. Cockburn**, J.H. Park***, E.Beyne, I. De Wolf, K.Croes, IMEC, *Sony Corporation, **Applied Materials Belgium, ***Applied Materials

5C.6 Effect of TSV Presence on FEOL Yield and Reliability, T. Kauerauf, A. Branka, K. Croes, A. Redolfi, Y. Civale, C. Torregiani, G. Groeseneken, E. Beyne, IMEC

SESSION 5D: TRANSISTORS

5D.1 Self-heat Reliability Considerations on Intel's 22nm Tri-Gate Technology, C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C.-H. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai, P. Vandervoorn, Intel Corporation

5D.2 Bias Temperature Instability and Hot Carrier Circuit Ageing Simulations Specificities in UTBB FDSOI 28nm Node, D. Angot, V. Huard, X. Federspiel, F. Cacho, A. Bravaix*, STMicroelectronics and *IM2NP-ISEN

5D.3 Investigation of Self-Heating Effect Induced Hot-Carrier-Injection Stress Behaviors in High-Voltage Power Devices, Y.H. Huang, L.Y. Leu, C.-C. Liu, Y-H. Lee, J.S. Wang, A. Mehta, K. Wu, H-T. Lu, P-C. Su, J-P. Chiang, H-L. Chou, Y-C. Jong and H-C. Tuan, TSMC

5D.4 Channel Hot-Carriers Degradation in MOSFETs: A Conductive AFM Study at the Nanoscale, A. Bayerl, M.Porti, J. Martin-Martinez, M. Lanza, R. Rodriguez, V. Velayudhan, E. Amat, M. Nafria, X. Aymerich, M.B. Gonzalez*,, E. Simoen**, Universitat Autònoma de Barcelona,*CNM, ** IMEC

SESSION 5E: MEMORIES

5E.1 Resistance Instabilities in a Filament-Based Resistive Memory (Invited), F.T. Chen, H.-Y. Lee, Y.-S. Chen, S.Z. Rahaman, C.-H. Tsai, K.-H. Tsai, T.-Y. Wu, W.-S. Chen, P.-Y. Gu, Y.-D. Lin, S.-S. Sheu, M.-J. Tsai, L.-H. Lee, T.-K. Ku, P.-S. Chen*, Industrial Technology Research Institute, *Minghsin University of Science and Technology

5E.2 Investigation of the Role of Electrodes on the Retention Performance of HfO_x based RRAM Cells by Experiments, Atomistic Simulations and Device Physical Modeling, B. Traore, K. Xue, E. Vianello, G. Molas, P. Blaise, B. De Salvo, A. Padovani*, O. Pirrotta*, L. Larcher*, L. Fonseca**, Y. Nishi***, CEA-LETI, *Università di Modena e Reggio Emilia, **State University of Campinas, ***Stanford University

5E.3 Microscopic Origin of Random Telegraph Noise Fluctuations in Aggressively Scaled RRAM and its Impact on Read Disturb Variability, N. Raghavan, R. Degraeve, A. Fantini, L. Goux, S. Strangio, B. Govoreanu, D. Wouters, G. Groeseneken, M. Jurczak, IMEC

5E.4 Investigation of the Impact of the Oxide Thickness and RESET Conditions on Disturb in HfO2-RRAM integrated in a 65nm CMOS Technology, T. Diokh, E. Le-Roux, S. Jeannot, M. Gros-Jean, P. Candelier, J.F. Nodin*, V. Jousseaume*, L. Perniola*, H. Grampeix*, T. Cabout*, E. Jalaguier*, M. Guillermet*, B. De Salvo*, STMicroelectronics and *CEA-LETI

SESSION 6A: TECHNOLOGY/DEVICES BEYOND CMOS

6A.1 Reliable Micro-Electro-Mechanical (MEM) Switch Design for Ultra-Low Power Logic (Invited), H. Kam, Y. Chen*, T.-J. King Liu*, Intel Corporation, *University of California, Berkeley

6A.2 Reliability of Graphene Interconnects and N-type Doping of Carbon Nanotube Transistors (Invited), L. Liyanage, X. Chen, H. Wei, H.-Y. Chen, S. Mitra, H.S.P. Wong, Stanford University

6A.3 Tunnel Transistors for Energy Efficient Computing (Invited), S. Datta, R. Bijesh, H. Liu, D. Mohata, V. Narayanan, Pennsylvania State University

SESSION 6B: MEMS

6B.1 Wafer-Level MEMS Package and its Reliability Issues (Invited), S. Tanaka, M. Esashi, Tohoku University

6B.2 Key Improvements of the MEMS Switch Lifetime Thanks to a Dielectric-free Design and Contact Reliability Investigations in Hot/Cold Switching Operations, F. Souchon, B. Reig, C. Dieppedale, L. Thouy, A. Koszewski, H. Sibuet, G. Papaioannou*, CEA-LETI and *University of Athens

6B.3 Electrical Characterization of Un-doped Diamond Films for RF MEMS Application, L. Michalas, M. Koutsoureli, E. Papandreou, G. Papaioannou, S. Saada*, C. Mer*, R. Hugon*, P. Bergonzo*, A. Leuliet**, P. Martins**, S. Bansropun**, A. Ziaei**, National Kapodistrian University of Athens, *CEA,LIST Diamond Sensors Laboratory, ** Thales Research and Technology

6B.4 Characterization of Dielectric Charging and Reliability in Capacitive RF MEMS Switches, S. Kim, S. Cunningham, J. McKillop, A.Morris, WiSpry, Inc.

SESSION 6C: SOFT ERRORS

6C.1 Space Radiation and Reliability Qualifications on 65nm CMOS 600MHz Microprocessors (Invited), S. Clerc, F. Abouzeid, G. Gasiot, J.-M. Daveau, C. Bottoni, M. Glorieux, J.-L. Autran*, F. Cacho, V. Huard, L. Dugoujon, R. Weigand**, F. Malou***, L. Hili**, P. Roche, STMicroelectronics, *Aix-Marseille Universit and CNRS, **European Space Agency, and ***Centre National d’Etudes Spatiales

6C.2 Identification of Pulse Quenching Enhanced Layouts with Subbandgap Laser-Induced S ingle Event Effects, J. Ahlbin, N. Hooten*, M. Gadlage**, J. Warner***, S. Buchner***, D. McMorrow***, L. Massengill*, University of Southern California - Information Sciences Institute, *Vanderbilt University, **NAVSEA Crane,*** Naval Research Laboratory

6C.3 Impact of Cell Distance and Well-contact Density on Neutron-induced Multiple Cell Upsets, J. Furuta, K. Kobayashi*, H. Onodera, Kyoto University and *Kyoto Institute of Technology

6C.4 Impact of Parasitic Bipolar Action and Soft-Error Trend in Bulk CMOS at Terrestial Environment, T. Uemura, T. Kato, H. Matsuyama, Fujitsu Semiconductor, Ltd.

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S1-1 III-V Device Characterization, Suman Datta, Penn State Univ.

S1-2 Monte Carlo Methods in Reliability Physics, John Evans, NASA

S1-3 Fundamentals of RTN, BTI, and Hot Carrier Degradation: A Matter of Timescales,
Tibor Grasser, Technische Universitaet Wien

S1-4 Fundamentals of Dielectric Breakdown Reliability, Ernest Wu and Jordi Suñé* ,
IBM SRDC, Universitat Autonoma de Barcelona

S2-1 Reliability Physics of High-k/Metal Gate Stacks for Advanced CMOS Technology,
Eduard Cartier, IBM

S2-2 Metal Gate/High-k Bias Temperature Instability: Characterization and Modeling,
Andreas Kerber, GLOBALFOUNDRIES

S2-3 High-k / Metal Gate 3 (TDDB), Thomas Kauerauf, imec

S2-4 Emerging Middle-of-line Reliability Issues, Fen Chen, IBM Microelectronics

S3-1 In-Situ Monitoring of Reliability in Circuits, Chris H. Kim,
University of Minnesota – Twin Cities

S3-2 Reliable systems from unreliable components: Resilient and adaptive circuits,
Jim Tschanz, Intel

S3-3 Starter Kit for Chip-to-System Reliability, Mohammad Tehranipoor, Nematollah
Bidokhti, Bill Eklow, University of Connecticut, Cicso Systems

S3-4 Design for Reliability, Vincent Huard, STMicroelectronics

S4-1 Flash Reliability, Todd Marquart, Micron

S4-2 Emerging Memory Technologies, Matthew Marinella, Sandia

S4-3 On the Intrinsic Variability and Reliability of Solar Cells, Muhammad A. Alam,
Purdue University

S4-4 Reliability of SiC Power MOSFETs, Aivars Lelis, ARL – PRESENTATION NOT AVAILABLE

Monday Tutorials

M1.1 CMOS BEOL Metal Reliability (Electromigration & Stressmigration), Ki-Don Lee, Texas Instruments, Inc.

M1.2 Reliability of Package-Level Interconnects, Christine Hau-Riege, Qualcomm

M1.3 Chip-Package Interaction, Ingrid De Wolf, imec and KU Leuven

M2.1 Tri-gate Reliability, Steve Ramey, Intel

M2.2 Reliability of Beyond/Extended CMOS Devices, Ahmad Ehteshamul Islam, Air Force Research Laboratory

M2.3 Reliability of low-*k* interconnect dielectrics, Gaddi S. Haase, Sandia National Labs

M3.1 CMOS Reliability: From Discrete Device Degradation to Circuit Aging, Tanya Nigam, GLOBALFOUNDRIES

M3.2 The Implementation of Reliability Considerations in Simulation Tools, Ahmed Ramadan, Mentor Graphics

M3.3 Logic Soft Errors, Bharat Bhuva, Vanderbilt University

M4.1 Electronic Characterization of Defects in III-Nitride Materials and Devices, Steven A. Ringel, The Ohio State University

M4.2 Reliability of Power GaN HEMTs, Sameh G. Khalil, HRL

M4.3 GaN on SiC Degradation Modes and Reliability Evaluation, Jose Jimenez, TriQuint