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CD-6 Generation of Traps in AlGaN/GaN HEMTs During RF-and DC-Stress Test, M. Caesar, M. Dammann, V. Polyakov, P.Waltereit, W. Bronner, M. Baeumler, R. Quay, M. Mikulla, O. Ambacher, Fraunhofer Institute for Applied Solid-State Physics

CD-7 Clarification of the Degradation Modes of an InP-Based Semiconductor MZ Modulator, H. Mawatari, T. Yasui, K. Watanabe, M. Ishikawa, E. Yamada, Y. Shibata, H. Ishii, NTT Corporation

CP – CHIP-PACKAGE INTERACTION

CP-1 On the Temperature Dependence of Critical Moisture Concentration on Delamination Initiation in Microelectronic Devices, P. Alpern, K. C. Lee*, D. Lee*, M. P. J. Gowda, Infineon Technologies AG, *Infineon Technologies Asia Pacific Pte Ltd.

CR – CIRCUITS RELIABILITY

CR-1 Impacts of Random Telegraph Noise on FinFET Devices, 6T SRAM Cell, and Logic Circuits, M.-L. Fan, V. Pi-Ho Hu, Y.-N. Chen, P. Su, C.-T. Chuang, National Chiao Tung University

CR-2 Understanding the Impact of Transistor-Level BTI Variability, J. Fang, S. Sapatnekar, University of Minnesota

CR-3 SPICE Simulations of Data Path Timing Margins after Dielectric Breakdown from Gate-to-Drain using Accurate Equivalent Circuit Models, R. T. Cakici, P. E. Nicollian, C. A. Chancellor, Texas Instruments Incorporated

CR-4 Reliability Study Under DC Stress on mmW LNA, Mixer and VCO, S. Ighilahriz, F. Cacho, L. Moquillon, S. Razafimandimby, F. Blanchet, J. Morelle, N. Corrao*, V. Huard, C. Arnaud, P. Garcia, P. Benech*, J.-M. Fournier*, STMicroelectronics, *IMEP-LAHC

CR-5 Net-Level Reliability Analysis for Interconnect Self-Heat, L. Jiang, D. Pantuso, A. Schmitz, J. Thomas, Intel Corporation

EL – ESD AND LATCHUP

EL-1 Abnormal ESD Failure Mode with Low-Voltage Turn-on Phenomenon of LDMOS Output Driver, J. Park, M. Orshansky, The University of Texas at Austin

EL-2 The Failure Mechanism Re-Investigation of ESD Device On EPI Wafer, J.-H. Lee, C. Kung, E. Kung, J.-R. Shih*, Real Test Company, *Taiwan Semiconductor Manufacturing Company

EL-3 ESD Protection Structure with Inductor-Triggered SCR for RF Applications in 65-nm CMOS Process, C.-Y. Lin, L.-W. Chu, M.-D. Ker, M.-H. Song*, C.-P. Jou*, T.-H. Lu*, J.-C. Tseng*, M.-H. Tsai*, T.-L. Hsu*, P.-F. Hung*,T.-H. Chang*, National Chiao-Tung University, *Taiwan Semiconductor Manufacturing Company

EM – ELECTROMIGRATION/VOIDING

EM-1 Copper Electromigration Failure Times Evaluated Over a Wide Range of Voiding Phases, Y. Li, K. Croes, T. Kirimura*, Y. K. Siew, Z. Tőkei, IMEC, *Fujitsu Semiconductor Europe

EM-2 Optimization of NH_3 Plasma Surface Treatment Using Cu Silicide Formation for EM/SM Improvement, W.-C. Baek, N. Chowdhury, L. Loi, H.-S. Kim, S. Kim, A. del Rosario, E. Adem, B. Tracy, J. Pak, Spansion Inc.

EM-3 Grain Structure Analysis and Implications on Electromigration Reliability for Cu Interconnects, L. Cao, K. J. Ganesh, L. Zhang, P. Ferreira, P. Ho, The University of Texas at Austin

EM-4 Reliability Evaluations of ECP Tools and Chemistries, G. Hall, D. Allman, G.Piatt, P. Hulse, ON Semiconductor

EM-5 A Novel Degradation Mechanism in SiCr-O Based Thin Film Resistors Under Temperature and Current Stress, Y. Li, P. Huiskamp, NXP Semiconductors

EM-6 Reliability Assessment and Physical Failure Analysis of Nanoscale Hard-Mask-Etching Al Interconnect, M.-Y. Lee, A. S. Teng,C.-H. Tu, L.-K. Kuo,S.-Q. Dai, C. C. Shine, T.C. Yen, H.-J. Lee, C.-Y. Lu, Macronix International Co., Ltd.

EM-7 Investigation on Physical Origins of Endurance Failures in PRAM, J. Bae, K. Hwang, K.H. Park, S. Jeon, J. Choi, J. Ahn, S. Kim, D.-h. Ahn, H. Jeong, S. Nam, G. Jeong, H.K. Cho, D.-h. Jang*, C.-G. Park*, Samsung Electronics Co., Ltd., *POSTECH

EM-8 Critical Temperature Shift for Stress Induced Voiding in Advanced Cu Interconnects for 32 nm and Beyond, R. Morusupalli, R. Rao*, T.-K. Lee, Y.-L. Shen**, M. Kunz^, N. Tamura^, A. Budiman^^, CISCO Systems, *Vitesse Semiconductor Corp., **University of New Mexico, ^ALS, ^^LANL

FA – FAILURE ANALYSIS

FA-1 The Case Study of Poly-Silicon Grain Size and Resistance, P. Chou, United Microelectronics Corporation, Ltd.

FA-2 Improving Defect Localization Techniques with Laser Beam with Specific Analysis and Set-up

Modules, R. Llido, J. Gomez, V. Goubier, G. Haller, V. Pouget*, D. Lewis*, STMicroelectronics, *Université de Bordeaux

FA-3 A Study of the Influence of Electron Beam on Electrical Characteristics of LOCOS Device, H. S. Lin, C. H. Chao, United Microelectrics Corporation

FA-4 Enhancing Current Leakage Path Using a Novel Dual Source Heating System, H. S. Lin, J. Ma,United Microelectronics Corporation, Ltd.

FA-5 Real-Time Variation Mapping for Parametric Defect Localization on ICs: Proof of Concept, Improvements, and Application to New Parameters, L. Saury, S. Cany, ST-Ericsson

FA-6 Soft Defect Localization (SDL) Applied on Analog and Mixed-mode ICs Failure Analysis, J. Li, C. Wu, Freescale Semiconductor (China) Limited

GD – Gate Dielectrics

GD-1 The Amplitude of Random Telegraph Noise: Scaling Implications, K. P. Cheung, J. P. Campbell, S. Potbhare, A. Oates*, NIST, *TSMC

GD-2 Gate Stack Process Optimization for TDDB Improvement in 28nm High-k/Metal Gate nMOSFETs, K. T. Lee, H. Kim, J. Park, J. Park, Samsung Electronics

GD-3 A Comparative Study of Gate Stack Material Properties and Reliability Characterization in MOS Transistors with Optimal ALD Zirconia Addition for Hafina Gate Dielectric, C.-K. Chiang, J.C. Chang, W.H. Liu, C.C. Liu, J.F. Lin, C.L. Yang, J.Y. Wu, C.K. Chiang*, S.J. Wang*, United Microelectronics Corporation, *National Cheng Kung University

GD-4 Min-Log Approach to Modeling Dielectric Breakdown Data, E. Yashchin, B. Li*, J. Stathis, E. Wu*, IBM Research Division, *IBM Systems and Technology Group

GD-5 From Post-Breakdown Conduction to Resistive Switching Effect in Thin Dielectric Films, E. Miranda, D. Jimenez, J. Suñe, Universitat Autònoma de Barcelona

GD-6 Effects of Gate Process on NBTI Chracteristics of TiN Gate FinFET, J. J. Kim, M. Cho*, L. Pantisano*, T. Chiarella*, M. Togo*, N. Horiguchi*, G. Groeseneken*, B. H. Lee, Gwangju Institute of Science and Technology, *IMEC

GD-7 New Insights into Gate-Dielectric Breakdown by Electrical Characterization of Interfacial and Oxide Defects with Reverse Modeling Methodology, Y. M. Randriamihaja, D. Garetto, V. Huard, D. Rideau, D. Roy, M. Rafik, A. Bravaix*, STMicroelectronics, *ISEN-IM2NP

ME – Thermo-mechanical/MEMS

ME-1 On the Electro-Mechanical Reliability of NEMFET as an Analog/Digital Switch, A. Jain, A. E. Islam*, M. A. Alam, Purdue University, *University of Illinois Urbana-Champaign

ME-2 Charge Collection Mechanism in MEMS Capacitive Switches, M. Koutsoureli, L. Michalas, G. Papaioannou, University of Athens

ME-3 Design and Analysis of Anchorless Shuttle Nano-Electro-Mechanical Non-Volatile Memory for

High Temperature Applications, R. Vaddi, T. T Kim, V. Pott*, J.T.M. Lin*, Nanyang Technological University, *Institute of Microelectronics, *A*STAR

MY – MEMORY

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MY-2 Current Overshoot During Set and Reset Operations of Resistive Switching Memories, A. Chen, GLOBALFOUNDRIES

MY-3 Total Ionizing Dose Effects on Ultra Thin Buried Oxide Floating Body Memories, N. Mahatme, R. Schrimpf, R. Reed, B. Bhuva, A. Griffoni*#, E. Simeon*, M. Aoulaiche*, M. Jurczak*, D. Linten*, G. Groeseneken*, Vanderbilt, *IMEC, #now with OSRAM

MY-4 Improvement of Endurance Degradation for Oxide Based Resistive Switching Memory Devices Correlated with Oxygen Vacancy Accumulation Effect, Y. Lu, B. Chen, B. Gao, Z. Fang*, Y. Fu, J.Q. Yang, L. Liu, X. Liu, H. Yu*, J. Kang, Peking University, *Nanyang Technological University

MY-5 Comprehensive Modeling of NAND Flash Memory Reliability: Endurance and Data Retention, Z. Xia, D. S. Kim, N. Jeong, Y.-Gu Kim, J.-H. Kim, K.-H. Lee, Y.-K. Park, C. Chung, Samsung Electronics Co., Ltd.

PI – PROCESS INTEGRATION/3D/TSV

PI-1 Improved Reliability of Al_2O_3/InGaAsInP MOS Structures Through In-Situ Forming Gas Annealing, R. O'Connor, K. Cherkaoui, R. Nagle, , M. Schmidt, , I. Povey, M. Pemble, P. Hurley, University College Cork Lee Maltings

PI-2 Volcano Effect in Open Through Silicon via (TSV) Technology, J. Kraft, E. Stückler, C. Cassidy, W. Niko, F. Schrank, E. Wachmann, C. Gspan*, F. Hofer*, Austriamicrosystems AG, *Graz University of Technology

PV – PHOTOVOLTAIC DEVICES

PV-1 Analyzing Life Tests of CIS Solar Modules for Degradation Modeling, Y. Okuda, Solar Frontier K.K.

SE – SOFT ERRORS

SE-1 SET Pulse-Width Measurement Eliminating Pulse-Width Modulation and Within-Die Process Variation Effects, R. Harada, Y. Mitsuyama*, M. Hashimoto, T. Onoye, Osaka University, *Kochi University of Technology

SE-2 Temperature Dependence of Soft Error Rate in Flip-Flop Designs, S. Jagannathan, Z. Diggins, N. Mahatme, D. Loveless, B. Bhuva, S.-J. Wen*, R. Wong*, L.Massengill, Vanderbilt University, *Cisco Systems, Inc.

SE-3 Neutron-Induced Soft Error Analysis in MOSFETs from a 65nm to a 25 nm Design Rule using

Multi-Scale Monte Carlo Simulation Method, S.-i. Abe, Y. Watanabe, N. Shibano*, N. Sano*, H. Furuta**, M. Tsutsui**, T. Uemura**, T. Arakawa**, Kyushu University, *University of Tsukuba, **STARC

SE-4 Impact of Well Contacts on the Single Event Response of Radiation-Hardened 40 nm Flip-Flops, I. Chatterjee, S. Jagannathan, D. Loveless, B. Bhuva, S.-J. Wen*, R. Wong*, M. Sachdev**, Vanderbilt University, *Cisco Systems, **CertiChip Inc.

SE-5 Evaluation of Parasitic Bipolar Effects on Neutron-Induced SET Rates for Logic Gates, J. Furuta, R. Yamamoto*, K. Kobayashi*, H. Onodera, Kyoto University, *Kyoto Institute of Technology

XT – TRANSISTORS/TFTS

XT-1 Spectroscopic Charge Pumping in the Presence of High Densities of Bulk Dielectric Traps, J. Ryan, R. Southwick, J. Campbell, K. Cheung, C. Young, J. Suehle, NIST

XT-2 Evidence for P_b Center-Hydrogen Complexes After Subjecting PMOS Devices to NBTI Stress – A Combined DCIV/SDR Study, T. Aichinger, P.M. Lenahan, T. Grasser*, G. Pobegen**, M. Nelhiebel^, Pennsylvania State University, *TU Vienna, **KAI, ^Infineon

XT-3 A Comprehensive and Critical Assesment of 2-Stage Energy Level NBTI Model, S. Gupta, B. Jose, K. Joshi, A. Jain*, M.A. Alam*, S. Mahapatra, IIT Bombay, *Purdue University

XT-4 Correlation of 1/*f* Noise and High-Voltage-Stress-Induced Degradation in LDMOS, I. Mahmud, Z. Celik-Butler, P. Hao*, P. Srinivasan*, F. Hou*, B. Amey*, X. Cheng**, S. Pendharkar*, W. Huang**, University of Texas at Arlington, *Texas Instruments Inc., **Freescale Semiconductor Inc.

XT-5 Correlation of Single Trapping and Detrapping Effects in Drain and Gate Currents of Nanoscaled nFETs and pFETs, M. Toledano-Luque, B. Kaczer, E. Simoen, R. Degraeve, J. Franco, P.J. Roussel, T. Grasser*, G. Groeseneken, IMEC, *TU Wien

XT-6 Organic Thin Film Transistor Degradation Under Sunlight Exposure, N. Wrachien, A. Cester, D. Bari, G. Meneghesso, J. Kovac*, J. Jakabovic*, D. Donoval*, University of Padova, *Slovak University of Technology

XT-7 Analysis of the Threshold Voltage Turn-Around Effect in High-Voltage n-MOSFETs Due to Hot-Carrier Stress, I. Starkov, H. Enichlmair*, S. Tyaginov, T. Grasser, Vienna University of Technology, *Austriamicrosystems AG

XT-8 On the Frequency Dependence of the Bias Temperature Instability, T. Grasser, B. Kaczer*, H. Reisinger**, P. Wagner, M. Toledano-Luque*, TU Wien, *IMEC, **Infineon

XT-9 Positive Bias Temperature Instability Induced Positive Charge Generation in P+ Poly/SiON pMOSFET's, H. Park, P. E. Nicollian, V. Reddy, Texas Instruments Incorporated

XT-10 On the Microscopic Limit of the Modified Reaction-Diffusion Model for the Negative Bias Temperature Instability, F. Schanovsky, T. Grasser, TU Wien

XT-11 Physical Understanding and Modelling of new Hot-Carrier Degradation Effect on PLDMOS Transistor, S. Aresu, R.-P. Vollertsen, R. Rudolf, C. Schlünder, H. Reisinger, W. Gustin, Infineon

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XT-12 The Energy of Distribtuion of NBTI-induced in the Si Band Gap in PNO MOSFETs Hole Traps, X. Ji, Y. Liao, F. Yan, Y. Shi, G. Zhang*, Q. Guo*, Nanjing University, *Semiconductor Manufactory International Corporation

XT-13 Intrinsic Hot-Carrier Degradation of nMOSFETs by Decoupling PBTI Component in 28nm High-k/Metal Gate Stacks, N. H.-H. Hsu, J.-W. You, H.-C. Ma, S.-C. Lee, E. Chen, L. S. Huang, Y.-C. Cheng, O. Cheng, I.C. Chen, United Microelectronics Corporation Ltd.

XT-14 Detailed Study of Fast Transient Relaxation of Vt Instability in HKMG nFETs, K. Zhao, J. Stathis, E. Cartier, M. Wang, H. Jagannathan, S. Zafar, IBM T.J. Watson Research Center

XT-15 Hot Carrier Degradation: From Defect Creation Modeling to Their Impact on NMOS Parameters, Y. Mamy Randriamihaja, A. Zaka, V. Huard, M. Rafik, D. Rideau, D. Roy, A. Bravaix*, P. Palestri**, STMicroelectronics, *ISEN-IM2NP, **University of Udine