

2005
IEEE
International
Reliability
Physics
Symposium
Proceedings
43nd Annual

San Jose, California • April 17–21, 2005

Sponsored by
the IEEE Electron Devices Society and
the IEEE Reliability Society

2005 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

SYMPOSIUM OFFICERS

GENERAL CHAIR T.A. Rost, Texas Instruments
VICE GENERAL CHAIR C.D. Graas, IBM
SECRETARY B. Kiang, TSMC
FINANCE S. Krishnan, Texas Instruments

SYMPOSIUM COMMITTEE CHAIRS

TECHNICAL PROGRAM E.I. Cole, Jr., Sandia National Labs
PUBLICITY P.F. Bechtold, Agere Systems
REGISTRATION T.M. Moore, Omniprobe
ARRANGEMENTS D.L. Barton, Sandia National Labs
AUDIO-VISUAL R.C. Laco, The Aerospace Corporation
PUBLICATIONS J.H. Stathis, IBM Research
EXHIBITS G.B. Alers, Novellus Systems
TUTORIAL J.S. Suehle, NIST
WORKSHOPS C.R. Messick, Northrop Grumman
CONSULTANT R.C. Walker, SAR Associates
CONSULTANT D.F. Barber, Scien-Tech Associates

BOARD OF DIRECTORS

B.M. Pietrucha, Chair
Rowan University

C.D. Graas IBM	N.R. Mielke Intel	E.S. Snyder AMIS
L.A. Kasprzak Dade Behring Inc.	T. A. Rost Texas Instruments	A.G. Street QUALCOMM
J.W. McPherson Texas Instruments	H.A. Schafft NIST	W.R. Tonti IBM

PUBLISHED BY
THE ELECTRON DEVICE SOCIETY AND THE RELIABILITY SOCIETY
OF THE
INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limits of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved. Copyright © 2005 by the Institute of Electrical and Electronics Engineers, Inc.

IEEE Catalog No. 05CH37616
ISBN: 0-7803-8803-8 Softbound Edition
Library of Congress Number: 82-640313

PREFACE

by Tim Rost, 2005 IRPS General Chair

It is truly my pleasure to present the 43rd edition of the IRPS proceedings for your reference. The technical information contained in this volume is the culmination of the efforts of many people, most notably the authors whose work has been selected for publication and is described in detail in the pages that follow. This year we had a record number of submissions, from which a record number of papers were selected. The papers in this volume and their presentation at the Symposium represent the core focus of the IRPS.

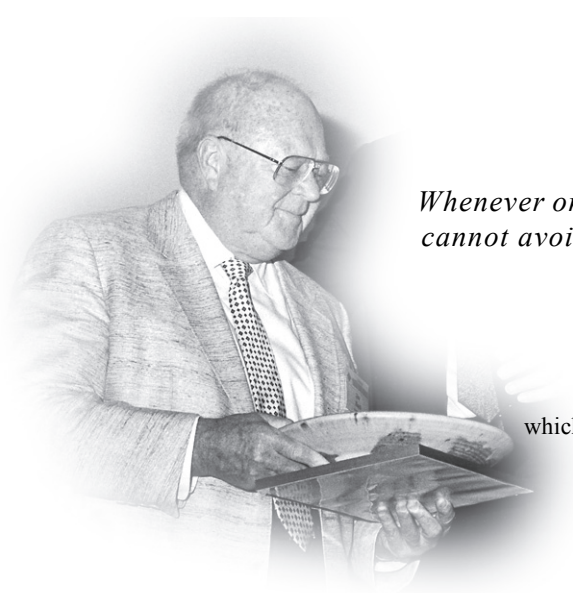
These proceedings also represent the efforts of many IRPS technical and management committee members who volunteer their time and energy, along with help from consultants, to help make the IRPS the leading forum for publishing, presenting, and discussing recent understanding in the broad area of microelectronics reliability. To the authors, volunteers, and consultants, I give my thanks for helping make the IRPS an annual success.

This year we have two presentations that I would like to call to your attention. David Yen, from Sun Microsystem's Scalable Systems Group will deliver the Symposium's keynote address. David's presentation is titled "Chip Multithreading Processors Enable Reliable High Throughput Computing" which describes the union of performance and reliability in state of the art microprocessor designs.

The other important presentation is a retrospective on Jim Black, presented by Jim Lloyd from IBM. Jim Black was a regular attendee at the IRPS and his foundational work on electromigration has had a profound and long-lasting effect on the semiconductor industry. In his honor, and due to his contributions to the IRPS and the reliability community at large, we are reprinting what is considered to be a foundational paper from the 1967 IRPS titled "*Mass Transport of Aluminum by Momentum Exchange with Conducting Electrons*" that outlines the basics of electromigration physics including the now-familiar Black's Law.

The CDROM companion to the proceedings, which you received as part of your registration package, contains files where color is used which can make viewing data graphs and charts a little easier. Abstracts of the Sunday and Monday tutorials can also be found on the last two pages of these proceedings.

A virtual IRPS 2005 on DVD-ROMs will be available soon after the Symposium (check www.irps.org for availability) that contains video, audio, and presentation material for all of the technical presentations. We hope that you enjoy this Symposium and will consider joining us again at another IRPS.



Jim Black

Whenever one thinks of electromigration failure in integrated circuits, one cannot avoid thinking of "Black's Law"

$$MTF = \frac{1}{A} \frac{1}{j^2} e^{(\phi/kT)}$$

which appeared in *J.R. Black, Proc. 6th Ann. Rel. Phys. Sym., 148 (1967)*

or for those of us who were lucky enough to have known him, of Jim Black himself. His cherubic countenance, sense of humor and modest manner belies the huge effect that his presence and pioneering work had on our community.

Jim didn't discover electromigration, that honor belongs to an otherwise obscure French scientist by the name of Gerardin a century before, nor did he explain the physics of electromigration, an honor shared by a number of scientists over the past few decades. However, Jim did look at the strange and troubling "cracked stripe" failures that

had begun to plague the fledgling semiconductor industry and threaten it with extinction before it reached puberty. His pioneering engineering approach to the subject gave us more than Black's Law.

MASS TRANSPORT OF ALUMINUM BY MOMENTUM EXCHANGE WITH CONDUCTING ELECTRONS

James R. Black
Motorola Inc.
Phoenix, Arizona

It is remarkable how many important topics were covered in this initial paper.

- 1) Effect of step coverage on electromigration lifetime
- 2) Hillock and whisker formation
- 3) Effect of texture
- 4) Grain size effects
- 5) Temperature dependence
- 6) Current density dependence

From his analysis, it was determined that electromigration in the wide Al films of the day was via a grain boundary diffusion mechanism. Also that well ordered large grained films are much superior to randomly oriented fine grained films. Most of these findings were rediscovered again and again over the years.

A non-scientific survey of the citation index shows that references to Black's Law have continued unabated since the original publication. If you count references to the three papers by Jim that are usually used to refer to it, we see at least 350 references. This does not count the many times it is mentioned without reference. It

has become such an accepted part of our vocabulary that many workers in the field apparently don't see the need to cite the reference. This is not a slight, but an honor.

In 1996 the MRS had a special session honoring 30 years of electromigration research and Jim, of course, was one of the most important contributors to be honored. He had been in retirement a few years and we convinced him to join the other honorees to present a paper. He was actually surprised that anybody remembered what he had done and was a bit taken aback by all the attention that was paid to him. I had the distinct honor and pleasure to be the chair of that session. I was sitting with Jim later during one of the normal sessions and he got to see many references to "Black's Law". He beamed and said "I can't believe it...they're still using that thing." But he was justifiably proud.

All we can do in our lives is to hope that we can have a beneficial effect, that we might have left it a little better for our presence than when we arrived. For all of us who were fortunate to have known him, we know he successfully realized that ambition.

Jim Lloyd

TABLE OF CONTENTS

INTERCONNECTS I

(Republished) Mass transport of aluminum by momentum exchange with conducting electrons <i>J.R. Black</i>	1
(Invited) The impact of scaling on interconnect reliability <i>C. Bruynseraede, Z. Tokei, F. Iacopi, G. P. Beyer, J. Michelon, and K. Maex</i>	7
Observation and restoration of negative electromigration activation energy behavior due to thermo-mechanical effects <i>Y.-J. Park, K.-D. Lee, and W.R. Hunter</i>	18
Impact of Via-Line contact on Cu interconnect electromigration performance <i>B. Li, J. Gill, C.J. Christiansen, T.D. Sullivan, and P.S. McLaughlin</i>	24
The impact of partially scaled metal barrier shunting on failure criteria for copper electromigration resistance increase in 65nm technology <i>K.-D. Lee, Y.-J. Park, and W.R. Hunter</i>	31
Stress migration and the mechanical properties of copper <i>G.B. Alers, J. Sukanto, P. Woytowicz, X. Lu, S. Kailasam, and J. Reid</i>	36

HIGH K DIELECTRICS

Single-electron emission of traps in HfSiON as high-k gate dielectric for MOSFETs <i>C.T. Chan, C.J. Tang, C.H. Kuo, H.C. Ma, C.W. Tsai, H. C.-H. Wang, M.H. Chi, and T. Wang</i>	41
Trap generation and progressive wearout in thin HfSiON <i>T. Kauerauf, R. Degraeve, F. Crupi, B. Kaczer, G. Groeseneken, and H. Maes</i>	45
PBTI & HCI characteristics for high-k gate dielectrics with Poly-Si & MIPS (Metal Inserted poly-Si) gates <i>H.-S. Jung, S.K. Han, M.J. Kim, J.P. Kim, Y.-S. Kim, H.J. Lim, S.J. Doh, J.H. Lee, M.Y. Yu, J.-H. Lee, N.-I. Lee, H.-K. Kang, S.G. Park, and S.B. Kang</i>	50
Interface states in HfO ₂ stacks with metal gate: Nature, passivation, generation <i>X. Garros, G. Reimbold, D. Duret, C. Leroux, B. Guillaumot, O. Louveau, C. Hobbs, and F. Martin</i>	55
High-K dielectrics breakdown accurate lifetime assessment methodology <i>G. Ribes, S. Bruyère, M. Denais, F. Monsieur, D. Roy, E. Vincent, and G. Ghibaudo</i>	61
Thermochemical understanding of dielectric breakdown in HfSiON with current acceleration <i>T. Yamaguchi, I. Hirano, R. Iijima, K. Sekine, M. Takayanagi, K. Eguchi, Y. Mitani, and N. Fukushima</i>	67
Interfacial layer dependence of HfSi _x O _y gate stacks on V _t instability and charge trapping using ultra-short pulse I-V characterization <i>C.D. Young, R. Choi, J.H. Sim, B.H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G.A. Brown, and G. Bersuker</i>	75

Comparison of NMOS and PMOS stress for determining the source of NBTI in TiN/HfSiON devices <i>H.R. Harris, R. Choi, B.H. Lee, C.D. Young, J.H. Sim, K. Mathews, P. Zeitzoff, P. Majhi, and G. Bersuker</i>	80
--	----

ESD

ESD induced damage on ultra-thin gate oxide MOSFETs and its impact on device reliability <i>A. Cester, S. Gerardin, A. Tazzoli, A. Paccagnella, E. Zanoni, G. Ghidini, and G. Meneghesso</i>	84
Interaction between electrostatic discharge and electromigration on copper interconnects for advanced CMOS technologies <i>D.K. Kontos, R. Gauthier, D.E. Ioannou, T. Lee, M. Woo, K. Chatty, C. Putnam, and M. Muhammad</i>	91
Study of factors limiting ESD diode performance in 90nm CMOS technologies and beyond <i>K. Chatty, R. Gauthier, C. Putnam, M. Muhammad, M. Woo, J. Li, R. Halbach, and C. Seguin</i>	98
Accurate prediction of the ESD robustness of semiconductor devices through physical simulation <i>C. Salaméro, N. Nolhier, M. Bafleur, and M. Zécri</i>	106

LATCHUP

The influence of a silicon dioxide-filled trench isolation structure and implanted sub-collector on latchup robustness <i>S.H. Voldman, E.G. Gebreselasie, L.W. Lanzerotti, T. Larsen, N.B. Feilchenfeld, S.A. St. Onge, A. Joseph, and J. Dunn</i>	112
Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger <i>M.-D. Ker and S.-F. Hsu</i>	121
Latchup in merged triple well structure <i>S.H. Voldman, E.G. Gebreselasie, M. Zierak, D. Hershberger, D.S. Collins, N.B. Feilchenfeld, S. A. St. Onge, and J. Dunn</i>	129
Latch-up in 65nm CMOS technology: A scaling perspective <i>G. Boselli, V. Reddy, and C. Duvvury</i>	137
Latchup and the domino effect <i>S.H. Voldman</i>	145

MEMORY I

(Invited) Reliability investigation for manufacturable high density PRAM <i>K. Kim and S.J. Ahn</i>	157
Reliability of 4Mbit MRAM <i>J. Akerman, P. Brown, D. Gajewski, M. Griswold, J. Janesky, M. Martin, H. Mekonnen, J.J. Nahas, S. Pietambaram, J.M. Slaughter, and S. Tehrani</i>	163
Novel soft erase and re-fill methods for a P+-POLY gate nitride-trapping non-volatile memory device with excellent endurance and retention properties <i>H.-T. Lue, Y.-H. Shih, K.Y. Hsieh, R. Liu and C.Y. Lu</i>	168
The kinetics of degradation of data retention of post-cycled NROM non-volatile memory products <i>M. Janai and B. Eitan</i>	175
Comparative reliability investigation of different nitride based local charge trapping memory devices <i>L. Breuil, L. Haspelslagh, P. Blomme, M. Lorenzini, D. Wellekens, J. De Vos, and J. Van Houdt</i>	181
Mechanism of drain disturb in SONOS flash EEPROMs <i>P.B. Kumar, R. Sharma, P.R. Nair, D.R. Nair, S. Kamohara, S. Mahapatra, and J. Vasi</i>	186

INTERCONNECTS II

Scaling effect on electromigration reliability for Cu/low-k interconnects <i>J.W. Pyun, X. Lu, S. Yoon, N. Henis, K. Neuman, K. Pfeifer, and P.S. Ho</i>	191
The dielectric material dependence of stress and stress relaxation on the mechanism of stress-voiding of Cu interconnects <i>J.-M. Paik, J.-K. Jung, and Y.-C. Joo</i>	195
Stress migration reliability of wide Cu interconnects with gouging vias <i>Y.K. Lim, R. Arijit, K.L. Pey, C.M. Tan, C.S. Seet, T.J. Lee, and D. Vigar</i>	203

SOFT ERRORS

Comparison of product failure rate to component soft error rate in a multi-core digital signal processor <i>X. Zhu, R. Baumann, C. Pilch, J. Zhou, J. Jones, and C. Cirba</i>	209
Radiation-induced clock jitter and race <i>N. Seifert, P. Shipley, M.D. Pant, V. Ambrose, and B. Gill</i>	215

A CMOS design style for logic circuit hardening <i>M. Zhang and N.R. Shanbhag</i>	223
A novel method for accurately estimating alpha-induced soft error rates <i>R. Takasu, Y. Tosaka, H. Fukuda, and Y. Kataoka</i>	230
MEMORY II	
(Invited) High-k materials for nonvolatile memory applications <i>J. Van Houdt</i>	234
Reliability assessment of discrete-trap memories for NOR applications <i>C.M. Compagnoni, D. Ielmini, A.S. Spinelli, A.L. Lacaita, and R. Sotgiu</i>	240
Bake enhanced erratic behavior in gate stress characteristics in flash memories <i>G. Tao, A. Scarpa, L. van Marwijk, and D. Dormans</i>	246
Impact of mechanical stress on interface trap generation in FLASH EEPROMs <i>A. Toda, S. Fujieda, K. Kanamori, J. Suzuki, K. Kuroyanagi, N. Kodama, Y. Den, and T. Nishizaka</i>	250
The effect of mechanical stress from stopping nitride to the reliability of tunnel oxide and data retention characteristics of NAND FLASH memory <i>J. Om, E. Choi, S. Kim, H. Lee, Y. Kim, H. Chang, S. Park, and G. Bae</i>	257
TRANSISTORS I	
Low frequency noise degradation in ultra-thin oxide (15Å) analog n-MOSFETs resulting from valence-band tunneling <i>J.W. Wu, J.W. You, H.C. Ma, C.C. Cheng, C.F. Hsu, G.W. Huang, C.S. Chang, and T. Wang</i>	260
Characterization and modeling of low frequency noise degradation due to NMOS hot electron stress <i>S. Dey and M. Agostinelli</i>	265
Anomalous NMOSFET hot carrier degradation due to trapped positive charge in a DGO CMOS process <i>D. Brisbin, Y. Mirgorodski, and P. Chaparala</i>	269
Hot carrier degradation on n-channel HfSiON MOSFETs: Effects on the device performance and lifetime <i>S. Cimino, L. Pantisano, M. Aoulaiche, R. Degraeve, D.H. Kwak, F. Crupi, G. Groeseneken, and A. Paccagnella</i>	275
FAILURE ANALYSIS I	
Dynamic thermal laser signal injection microscopy (T-LSIM) on AC propagation failures <i>M. LaPierre and R.A. Falk</i>	280
Advanced failure analysis of circuit-under-pad (CUP) structures in Cu/FSG and Cu/Low K technologies <i>H. Wu, V. Archer, S.M. Merchant, J. Cargo, D. Chesire, J. Antol, R. Mengel, J. Osenbach, S. Horvat, C. Peridier, and M. White</i> ..	286
Investigation on the thermal distribution of nMOSFETs under different operation modes by scanning thermal microscopy <i>E. Hendarto, A. Altes, R. Heiderhoff, J.C.H. Phang, and L.J. Balk</i>	294
Factors that influence ionic migration on printed wiring boards <i>M. Reid, J. Punch, B. Rodgers, M. J. Pomeroy, T. Galkin, T. Stenberg, O. Rusanen, E. Elonen, M. Vilèn, and K. Väkeväinen</i>	300
Delay variation mapping induced by dynamic laser stimulation <i>K. Sanchez, R. Deplats, F. Beaudoin, P. Perdu, D. Lewis, P. Vedagarbha, and G. Woods</i>	305
MEMS	
(Invited) Industry study on issues of MEMS reliability and accelerated lifetime testing <i>C. Fung</i>	312
Accelerating aging failures in MEMS devices <i>D.M. Tanner, J.A. Walraven, M.T. Dugger, T.B. Parson, S.A. Candelaria, M.W. Jenkins, A.D. Corwin, J.A. Ohlhausen, and E.M. Huffman</i>	317
Dynamic analysis and characterization of MEMS accelerometers by computational and opto-electromechanical methodologies <i>C. Furlong, R. Kok, and C.F. Ferguson</i>	325
Process-induced trapping of charge in PECVD dielectrics for RF MEMS capacitive switches <i>J.R. Webster, C.W. Dyck, C.D. Nordquist, J.A. Felix, M.R. Shaneyfelt, J.R. Schwank, and J.C.Banks</i>	330
The influence of the package environment on the functioning and reliability of RF-MEMS switches <i>W.M. van Spengen, P. Czarnecki, R. Puers, J.T.M. van Beek, and I. De Wolf</i>	337
Structural and thermal investigation for FBAR reliability in wireless applications <i>R.-Y. Fillit, B. Ivira, J. Boussey, R. Fortunier, and P. Ancey</i>	342

PRODUCT & CIRCUIT RELIABILITY I

Melt-segregate-quench programming of electrical fuse <i>T. Sasaki, N. Otsuka, K. Hisano, and S. Fujii</i>	347
Hot carrier generation and reliability of BT (body-tied) Fin type SRAM cell transistors ($W_{fin}=20\sim 70\text{nm}$) <i>Y.J. Ahn, H.J. Cho, H.S. Kang, C.-H. Lee, C. Lee, J. Yoon, T.Y. Kim, E.S. Cho, S.-K. Sung, D. Park, K. Kim, and B. Ryu</i>	352
Impact of proton irradiation on the RF performance of 0.12 μm CMOS technology <i>S. Venkataraman, B.M. Haugerud, E. Zhao, B. Banerjee, A. Sutton, P.W. Marshall, C.-H. Lee, J.D. Cressler, J. Laskar, J. Papapolymerou, and A.J. Joseph</i>	356

DIELECTRICS

Measurement and statistical analysis of single trap current-voltage characteristics in ultrathin SiON <i>R. Degraeve, B. Govoreanu, B. Kaczer, J. Van Houdt, and G. Groeseneken</i>	360
V_{ox}/E_{ox} -driven breakdown of ultra-thin SiON gate dielectric in p+gate-pMOSFET under low stress voltage of inversion mode <i>S. Tsujikawa, K. Shiga, H. Umeda, Y. Akamatsu, J. Yugami, Y. Ohno, and M. Yoneda</i>	366
Universality of power-low voltage dependence for TDDB lifetime in thin gate oxide PMOSFETs <i>K. Ohgata, M. Ogasawara, K. Shiga, S. Tsujikawa, E. Murakami, H. Kato, H. Umeda, and K. Kubota</i>	372
MVHR (Multi-Vibrational Hydrogen Release): Consistency with bias temperature instability and dielectrics breakdown <i>G. Ribes, S. Bruyère, M. Denais, D. Roy, and G. Ghibaudo</i>	377
Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification <i>B. Kaczer, V. Arkhipov, R. Degraeve, N. Collaert, G. Groeseneken, and M. Goodwin</i>	381
Change of acceleration behavior of time-dependent dielectric breakdown by the BEOL process: Indications for hydrogen induced transition in dominant degradation mechanism <i>T. Pompl, K.-H. Allers, R. Schwab, K. Hofmann, and M. Roehner</i>	388

PROCESS INTEGRATION RELIABILITY

Impact of plasma induced damage on PMOSFETs with TiN/Hf-silicate stack <i>S.C. Song, S.H. Bae, Z. Zhang, J.H. Sim, B. Sassman, G. Bersuker, P. Zeitzoff, and B.H. Lee</i>	398
--	-----

WIDE BANDGAP / COMPOUND DEVICES

Reliability considerations of strained silicon on relaxed silicon-germanium (SiGe) substrate <i>J.R. Shih and Kenneth Wu</i>	403
Reliability issues associated with operating voltage constraints in advanced SiGe HBTs <i>C.M. Grens, J.D. Cressler, J.M. Andrews, Q. Liang, and A.J. Joseph</i>	409
Hot electron stress degradation in unpassivated GaN/AlGaIn/GaN HEMTs on SiC <i>G. Meneghesso, R. Pierobon, F. Rampazzo, G. Tamiazzo, E. Zanoni, J. Bernat, P. Kordos, A.F. Basile, A. Chini, and G. Verzellesi</i> ..	415

PRODUCT & CIRCUIT RELIABILITY II

Impact of MOSFET gate-oxide reliability on CMOS operational amplifier in a 130-nm low-voltage CMOS process <i>J.-S. Chen and M.-D. Ker</i>	423
RF reliability subject to dynamic voltage stress in NMOS circuits <i>C. Yu and J.S. Yuan</i>	431
Reliability improvement and burn in optimization through the use of die level predictive modeling <i>W.C. Riordan, R. Miller, and E.R. St. Pierre</i>	435
Lifetime study for a poly fuse in a 0.35 μm polycide CMOS process <i>J. Fellner, P. Boesmueller, and H. Reiter</i>	446

LATE PAPERS

Characterization of thermoelectric devices in ICs as stimulated by a scanning laser beam <i>A. Glowacki and C. Boit</i>	450
New ballasting method for MOS output drivers and power bus clamps <i>E.R. Worley</i>	458
Testing to eliminate reliability defects from electronic packages <i>I. Memis</i>	462

BEOL DIELECTRICS

Breakdown characteristics of interconnect dielectrics <i>G.S. Haase, E.T. Ogawa, and J.W. McPherson</i>	466
Porosity content dependence of TDDB lifetime and flat band voltage shift by Cu diffusion in porous spin-on low-k <i>S.-S. Hwang, H.-C. Lee, H.-W. Ro, D.-Y. Yoon, and Y.-C. Joo</i>	474
Pseudo-breakdown phenomenon and barrier integrity in Cu/Porous ultra low-k damascene interconnects <i>Z. Chen, K. Prasad, N. Jiang, L.J. Tang, N. Babu, S. Balakumar, and C.Y. Li</i>	478
New approach of 90nm low-k interconnect evaluation using a voltage ramp dielectric breakdown (VRDB) test <i>O. Aubel, M. Kiene, and W. Yao</i>	483
Impact of buried capping layer on TDDB physics of advanced interconnects <i>K.Y. Yiang, W.J. Yoo, A. Krishnamoorthy, and L.J. Tang</i>	490
Role of dielectric and barrier integrity in reliability of sub-100 nm copper low-k interconnects <i>Z. Tokei, J. Van Aelst, C. Waldfried, O. Escorcica, P. Roussel, O. Richard, Y. Travalay, G.P. Beyer, and K. Maex</i>	495
Investigation of CVD SiCOH low-k time-dependent dielectric breakdown at 65nm node technology <i>F. Chen, K. Chanda, J. Gill, M. Angyal, J. Demarest, T. Sullivan, R. Kontra, M. Shinosky, J. Li, L. Economikos, M. Hoinkis, S. Lane, D. McHerron, M. Inohara, S. Boettcher, D. Dunn, M. Fukasawa, B.C. Zhang, K. Ida, T. Ema, G. Lembach, K. Kumar, Y. Lin, H. Maynard, K. Urata, T. Bolom, K. Inoue, J. Smith, Y. Ishikawa, M. Naujok, P. Ong, A. Sakamoto, D. Hunt, and J. Aitken</i>	501

ASSEMBLY & PACKAGING

Identification of new mechanism of epoxy underfill void formation in electronic packages <i>S.L.B. Dal and N.T. Zamora</i>	508
Influence of process parameters and bump geometry on the residual stress distribution in a chip-on-foil bonding process <i>P. Suter, R. Bauknecht, T. Graf, H. Duran, and I. Venter</i>	513
A study of electromigration failure in Pb-free solder joints <i>M. Ding, G. Wang, B. Chao, P.S. Ho, P. Su, T. Uehling, and D. Wontor</i>	518

TRANSISTORS II

A new drain voltage enhanced NBTI degradation mechanism <i>N.K. Jha, P.S. Reddy, and V.R. Rao</i>	524
Random charge effects for PMOS NBTI in ultra-small gate area devices <i>M. Agostinelli, S. Pae, W. Yang, C. Prasad, D. Kencke, S. Ramey, E. Snyder, S. Kashyap, and M. Jones</i>	529
The contribution of HfO ₂ bulk oxide traps to dynamic NBTI in pMOSFETs <i>B. Zhu, J.S. Suehle, E. Vogel, and J.B. Bernstein</i>	533
Negative bias temperature instability (NBTI) characteristics of bulk FinFETs <i>S.-Y. Kim, T. Park, J.-S. Lee, D. Park, K.-N. Kim, and J.-H. Lee</i>	538
Reliability investigation upon 30nm gate length ultra-high aspect ratio FinFETs <i>W.-S. Liao, S.-S. Chen, S. Chiang, and W.-T. Shiau</i>	541

HIGH VOLTAGE DEVICES

(Invited) Short and long term safe operating area considerations in LDMOS transistors <i>Philip L Hower and Sameer Pendharkar</i>	545
(ESREF Best Paper Invited) <i>Aresu S., De Ceuninck W., Van den bosch G., Groeseneken G., Moens P., Manca J., Wojciechowski D., Gassot P., "Evidence for source side injection hot carrier effects on lateral DMOS transistors", Microelectronics Reliability, Vol. 44, 2004, pp. 1621-1624. Presented paper ESREF2004 (Zurich)</i>	
Hot carrier degradation of lateral DMOS transistor capacitance and reliability issues <i>N. Hefyene, C. Anghel, R. Gillon, and A.M. Ionescu</i>	551
Electron trapping and interface trap generation in drain extended pMOS transistors <i>P. Moens, F. Bauwens, M. Nelson, and M. Tack</i>	555
Hot-carrier reliability in submicrometer 40V LDMOS transistors with thick gate oxide <i>J.F. Chen, K.-M. Wu, K.-W. Lin, Y.-K. Su, and S. L. Hsu</i>	560
Electrical characteristics and reliability of the extended drain voltage NMOS devices with the multi-RESURF junction <i>V.A. Vashchenko, D. Brisbin, P. Lindorfer, P. Chaparala, and P. Hopper</i>	565

Reliability assessment of deep trench isolation structures <i>P. Moens, P. Coppens, J. Baele, F. Bauwens, S. Boonen, H. De Vleeschouwer, F. De Pestel, and M. Tack</i>	573
---	-----

ASSEMBLY & PACKAGING POSTERS

A study of the reliability of MOSFETs in two stacked thin chips for 3D system in package <i>A. Ikeda, Y. Sugimoto, T. Kuwada, S. Kajiwara, T. Fujimura, K. Iwasaki, H. Ogi, A. Hamaguchi, H. Kuriyaki, R. Hattori, and Y. Kuroki</i>	578
Failure analysis of intermittent pin-to-pin short caused by phosphorous particle in molding compound <i>N. Wang, J. Wu, and S. Daniel</i>	580

BEOL DIELECTRICS POSTERS

Analysis of electric field distribution and its influence on dielectric failures in asymmetric copper interconnect structure <i>T.M.Z. Lin, W.M. Hsu, S.Y. Lee, C.C. Chiu, and K. Wu</i>	582
Electro-optical reliability characterization of advanced Cu/Low-K interconnects <i>C. Guedj, J.F. Guillaumond, F. Mondon, L. Arnaud, V. Arnal, G. Reimbold, and J.Torres</i>	584
Stability of capacitance voltage linearity for high-k MIM capacitor <i>C. Besset, S. Bruyere, F. Monsieur, S. Boret, E. Deloffre, and E. Vincent</i>	586
Fast reliability evaluation of backend dielectrics using lifetime prediction techniques at wafer level <i>C. Hong, L. Milor, M.Z Lin, W.M. Hsu, and Y. Peng</i>	588

WIDE BANDGAP / COMPOUND DEVICES POSTERS

Hot carrier reliability in GaAs PHEMT MMIC power amplifiers <i>Y.C. Chou, R. Grundbacher, R. Lai, G. P. Li, Q. Kan, M. Yu, L. Callejo, D. Leung, D. Eng, T. Block, and A. Oki</i>	590
Gate oxide reliability in 4H-SiC MOS devices <i>S. Krishnaswami, M. Das, B. Hull, S.-H. Rye, J. Schofield, A. Agarwal, and J. Palmour</i>	592

DIELECTRICS POSTERS

Direct tunneling stress-induced leakage current in nMOS devices with ultrathin gate oxides <i>P. Samanta, T.Y. Man, A.C.K. Chan, Q. Zhang, C. Zhu, and M. Chan</i>	594
A comprehensive solution for ultra-thin oxide reliability issue including a novel explanation of power-law exponent variations <i>T.-K. Kang, J. Shieh, O. Lo, J.-P. Chen, C.-L. Lin, and K.C. Su</i>	596
A new model for the post-breakdown conductance of MOS devices based on the generalized diode equation <i>E. Miranda</i>	598
Direct observation of trap behaviors during degradation and breakdown evolution in highly stressed SiO ₂ films by conductive atomic force microscopy <i>L. Zhang and Y. Mitani</i>	600
Exponential dependence of percolation resistance on gate voltage and its impacts on progressive breakdown <i>V.L. Lo, K.L. Pey, C.H. Tung, D.S. Ang, and L.J. Tang</i>	602
Device degradation model for stacked-ONO gate structure with using SONOS and MOS transistors <i>J.-H. Yi, J.-H. Ahn, H. Shin, Y.-J. Park, and H.S. Min</i>	604

ESD POSTERS

Design on power-rail ESD clamp circuit for 3.3-V I/O interface by using only 1-V/2.5-V low-voltage devices in a 130-nm CMOS process <i>M.-D. Ker, W.-Y. Chen, and K.-C. Hsu</i>	606
Significance of including substrate capacitance in the full chip circuit model of ICs under CDM stress <i>M.S.B.Sowariraj, P. de Jong, C. Salm, T. Smedes A.J.T. Moutaahan, and F.G Kuper</i>	608
Design and characterization of a novel high voltage power supply ESD protection <i>K. Reynders, P. Moens, D. Wojciechowski, and M. Tack</i>	610
ESD protection window targeting using LDMOS-SCR devices with PWELL-NWELL super-junction <i>V.A. Vashchenko and M. ter Beek</i>	612

FAILURE ANALYSIS POSTERS

Novel electrical re-connection of very thin fine pitch ball grid array (VFBGA) package for advanced backside fault isolation <i>L. Qian, Y. Xu, G. Song, and X. Ji</i>	614
---	-----

Study of silicon-nitride induced damage on thin gate oxide <i>W. Dong, J. Zhou, S. Liao, C. Niou, and W.T.K. Chien</i>	616
Failure analysis of pixel shorting problems in polymer light emitting diode (PLED) displays <i>L. Wu, A. Johnson, D. Kolosov, I. Parker, and J. Trujillo</i>	618
Physical mechanism of high resistance of tungsten plug as a root cause of low yield and reliability issue in deep-sub-micro Si technology <i>W. Zhang and K.T. Tan</i>	620
Investigation of localized breakdown spots in thin SiO ₂ using scanning capacitance microscopy <i>S.D. Wang, M.N. Chang, C.Y. Chen, and T. F. Lei</i>	622
Junction leakage induced by silicon dislocation in a 0.13 micron logic process <i>R. Chen, J.Y.C. Lin, W. Dong, A. Guo, S. Liao, C. Niou, and K.Chien</i>	624

HIGH K DIELECTRICS POSTERS

Effects of post metallization annealing on the electrical reliability of ultra-thin HfO ₂ Films with MoN and WN gate electrode <i>S. Chatterjee, Y. Kuo, J. Lu, J. -Y. Tewg, and P. Majhi</i>	626
Effects of optimized nitrogen tailoring in high-k dielectrics on impurity penetration and stress induced device degradation <i>C.Y. Kang, S.J. Rhee, C.H. Choi, M.S. Akvar, H.-S. Kim, M. Zhang, T. Lee, I. Ok, F. Zhu, and J.C. Lee</i>	628
Breakdown and conduction mechanisms of ALD HfSiON dielectric with TaN gate using carrier separation analysis <i>S.J. Doh, J.H. Lee, J.P. Kim, J.-H. Lee, Y.-S. Kim, H.-J. Lim, H.-S. Jung, S.K. Han, M.J. Kim, N.-I. Lee, H.-K. Kang, S.G Park, and S.B. Kang</i>	630
Influence of gate material and stress voltage on post breakdown leakage current of high k dielectrics <i>R. Duschl, M. Kerber, U. Schroeder, T. Hecht, S. Jakschik, C. Kapteyn, and S. Kudelka</i>	632
Threshold voltage instability of HFSIO dielectric MOSFET under pulsed stress <i>R. Choi, R. Harris, B.H. Lee, C.D. Young, J.H. Sim, K. Matthews, M. Pendley, and G. Bersuker</i>	634
Implication of polarity dependence degradation on NMOSFET with polysilicon/Hf-silicate gate stack <i>R. Choi, B.H. Lee, C.D. Young, J.H. Sim, K. Mathews, G. Bersuker, and P. Zeitzoff</i>	636
Comparison of hot carrier stress and constant voltage stress in Hf-silicate NMOS transistors with Poly and TiN gate stack <i>J.H. Sim, B.H. Lee, S.C. Song, C.D. Young, R. Choi, H.R. Harris, and G. Bersuker</i>	638
Effects of high-k post-deposition cleaning in improving CMOS bias instabilities and mobility: A potential issue in reliability of dual metal gate technology <i>M.S. Akbar, N. Moumen, J. Barnett, B.-H. Lee, and J.C. Lee</i>	640
Dominant SILC mechanisms in HfO ₂ /TiN gate nMOS and pMOS transistors <i>S.A. Krishnan, J.J. Peterson, C.D. Young, G. Brown, R. Choi, R. Harris, J.H. Sim, P. Zeitzoff, P. Kirsch, J. Gutt, H.J. Li, K. Matthews, J.C. Lee, B.H. Lee, and G. Bersuker</i>	642
Significant improvement in reliability of HFSION gate insulator <i>M. Inoue, J. Yugami, F. Fujita, K. Shiga, M. Mizutani, K. Nomura, J. Tsuchimoto, Y. Ohno, and M. Yoneda</i>	644
Effect of high pressure deuterium annealing on electrical and reliability characteristics of MOSFETs with high-k gate dielectric <i>H. Park, M.S. Rahman, M. Chang, B. Lee, M. Gardner, C.D. Young, and H. Hwang</i>	646
Charge trapping by oxygen-related defects in HfO ₂ -based high-k gate dielectrics <i>K. Yamabe, M.Goto, K. Higuchi, A. Uedono, K. Shiraishi, S. Miyazaki, K. Torii, M. Boero, T. Chikyow, S. Yamasaki, H. Kitajima, K. Yamada, and T. Arikado</i>	648

HIGH VOLTAGE DEVICES POSTERS

Reliability failures due to charge injection in SOI under high voltage conditions <i>H.J. Bruggers, I.M. Emmerik-Weijland, and R.T.H. Rongen</i>	650
Comprehensive study of postprocessed copper heat sinks on smart power drivers for thermal SOA improvement <i>G. Van den bosch, E. Driessens, T. Webers, B. Elattari, D. Wojciechowski, P. Gassot, P. Moens, and G. Groeseneken</i>	652
Effect of layout orientation on the performance and reliability of high voltage N-LDMOS in standard submicron logic STI CMOS process <i>B. Wang, H. Nguyen, J. Mavoori, A. Horch, Y. Ma, T. Humes, and R. Paulsen</i>	654

INTERCONNECTS POSTERS

Degradation of electromigration lifetime by post-annealing for Cu/Low-k interconnects <i>Y. Kakuhara and K. Ueno</i>	656
Determination of the acceleration factor between wafer level and package level electromigration test <i>X. Federspiel, D. Ney, and V. Girault</i>	658
Influence of diffusion barrier on reliability identification of diffusion paths in Cu/POROUS low K interconnect <i>J.F. Guillaumond, L. Arnaud, C. Guedj, V. Arnal, W.F.A. Besling, G. Reibold, M. Dupeux, and J.Torres</i>	660

MEMORY POSTERS

Method for endurance optimization of the HIMOS flash memory cell <i>T. Yao, A. Lowe, T. Vermeulen, N. Bellafiore, J. Van Houdt, and D. Wellekens</i>	662
A voltage acceleration lifetime model to predict post-cycling LTDR characteristics of split-gate flash memories <i>L.-C. Hu, A.-C. Kang, T.I. Wu, E. Chen, J.R. Shih, H.W. Chin, Y.-F. Lin, K. Wu, and Y.-C. King</i>	664
A highly reliable NAND structure flash memory capable for low voltage operation <i>Y.C. Lin, C.S. Lai, S.S. Chung, E. Yang, S. Pittikoun, S.-M. Tzeng, and C.C.-H. Hsu</i>	666
Dielectric engineering in nanocrystal memory devices for improved programming dynamics <i>J.J. Lee, W. Bai, and D.-L. Kwong</i>	668
Effect of STI shape and tunneling oxide thinning on cell Vth distribution in the flash memory <i>J.D. Lee, J.H. Kim, W. Lee, S.H. Lee, H.Y. Lim, J.D. Lee, S.W. Nam, H.D. Lee, and C.L. Song</i>	670

PRODUCT & CIRCUIT RELIABILITY POSTERS

How much mismatch should be simulated in the high density SRAM sense amplifier design <i>T. Peng</i>	672
Investigation into the correlation of wafer sort and reliability yield using electrical stress testing <i>A. Flynn and S. Millar</i>	674
Fast WLRC applications in foundry fabrication <i>S. Tseng, W.T.K. Chien, W. Wang, A. Zhao, and E. Gong</i>	676
Novel test chip for statistical evaluation of defect density and reliability of contacts and vias <i>A. Cabrini, D. Cantarelli, P. Cappelletti, R. Casiraghi, D. Iezzi, C. Lombardi, A. Maurelli, M. Pasotti, P.L. Rolandi, and G. Torelli</i>	678
Hot carrier effect on CMOS RF amplifiers <i>E. Xiao</i>	680
Estimating DPPM during the prototype to product ramp phase <i>T.J. Anderson</i>	682

PROCESS INTEGRATION RELIABILITY POSTERS

Gettering effect of high-dose arsenic implantation and boron diffusion on gate oxide integrity in trench isolated high voltage silicon-on insulator process <i>D.H. Lu, S. Jimbo, N. Fujishima, S. Wakimoto, and M. Ogino</i>	684
Reliability of MIM HAO capacitor for 70nm DRAM <i>K. Hong, D.-S. Kil, H.-K. Woo, J. Kim, H.-S. Song, K.-S. Park, S.-J. Yeom, H.-S. Yang, J.-S. Roh, H.-C. Sohn, J.-W. Kim, and S.-W. Park</i>	686
Copper via chain under etching process improvement <i>J. Ji, M. Zhang, W. Dong, A. Guo, S. Liang, S. Liao, C. Niou, and K. Chien</i>	688
Stress migration related reliability concerns <i>J.-Y. Ma, S.F.C. Tseng, K.W.T. Chien, and V.W.W. Ruan</i>	690

SOFT ERRORS POSTERS

Cancer radiotherapy equipment as a cause of soft-errors in electronic equipment <i>J.D. Wilkinson, C. Bounds, T. Brown, B. Gerbi, and J. Peltier</i>	692
A new neutron facility for single-event effect testing <i>A.V. Prokofiev, S. Pomp, J. Blomgren, O. Byström, C. Ekström, O. Jonsson, D. Reistad, U. Tippawan, D. Wessman, V. Ziemann, and M. Österlund</i>	694
Unfolding procedure for SER measurements using quasi-monoenergetic neutrons <i>M. Olmos, A. Prokofiev, and R. Gaillard</i>	696

TRANSISTORS POSTERS

Channel soft breakdown enhanced excess low-frequency noise in ultra-thin gate oxide PD analog SOI devices <i>S. Chiang, M.C. Chen, W.S. Liao, J.W. You, M.F. Lu, Y.S. Hsieh, W.M. Lin, S. Huang-Lu, W.T. Shiau, S.C. Chien, and T. Wang</i>	698
Impact of substrate bias on p-MOSFET negative bias temperature instability <i>S. Mahapatra, T.R. Dalei, P.B. Kumar, D. Vargheese, D. Saha, and M.A. Alam</i>	700
Mechanism of on-current and off-current instabilities under electrical stress in polycrystalline silicon thin-film transistors <i>S. De Wang, T.Y. Chang, W.H. Lo, and T.F. Lei</i>	702
A new finding on NBTI lifetime model and an investigation on NBTI degradation characteristic for 1.2nm ultra thin oxide <i>C.L. Chen, Y.M. Lin, C.J. Wang, and K. Wu</i>	704
New observations on the damage relaxation mechanisms in P-MOSFETs under dynamic NBTI stressing <i>D.S. Ang and S. Wang</i>	706
The energy driven paradigm of NMOSFET hot carrier effects <i>S.E. Rauch III and G. LaRosa</i>	708
Localization of NBT hot-carrier-induced oxide damage in SOI pMOSFET's <i>C.S. Lai, S.C. Hung, J.W. Lee, and S.S. Chung</i>	710
Physical mechanism of NBTI relaxation by RF and noise performance of RF CMOS devices <i>Z. Luo and J. P. Walko</i>	712
MOSFET asymmetry and gate-drain/source overlap effects on hot carrier reliability <i>S. Aur, S.-H. Yang, and T. Tran</i>	714
Biographies	716
Page Number Cross-reference to Session/Poster Paper #	754
2005 Committees	755
2003 Paper Awards	760
2005 Tutorial Program Abstracts	762

MARK YOUR CALENDAR AND START PLANNING TO ATTEND,
AND POSSIBLY
CONTRIBUTE A PAPER, TO THE FOLLOWING SYMPOSIA:

2006 INTERNATIONAL RELIABILITY PHYSICS
SYMPOSIUM
March 26-30, 2006
San Jose McEnery Convention Center / San Jose Marriott
San Jose, CA

2007 INTERNATIONAL RELIABILITY PHYSICS
SYMPOSIUM
Phoenix Civic Plaza Convention Center / Hyatt Regency Phoenix at Civic Plaza
April 15-19, 2007
Phoenix, AZ