



2003

IEEE

International

Reliability

Physics

Symposium

Proceedings

41st Annual

Dallas, Texas • March 30–April 4, 2003

**Sponsored by
the IEEE Electron Devices Society and
the IEEE Reliability Society**

IEEE Catalog No. 03CH37400

2003 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

SYMPOSIUM OFFICERS

GENERAL CHAIR E.S. Snyder, Sandia Technologies
VICE GENERAL CHAIR B.M. Pietrucha, Rowan University
SECRETARY C.R. Messick, Northrop Grumman
FINANCE E.I. Cole, Jr., Sandia National Labs

SYMPOSIUM COMMITTEE CHAIRS

TECHNICAL PROGRAM T.A. Rost, Texas Instruments
PUBLICITY G.B. Alers, Novellus Systems
REGISTRATION J.S. Suehle, NIST
ARRANGEMENTS T.M. Moore, Omniprobe
AUDIO-VISUAL S. Krishnan, Texas Instruments
PUBLICATIONS Y.A. Peng, TSMC
EXHIBITS R.C. Laco, The Aerospace Corporation
TUTORIAL D.L. Barton, Sandia National Labs
WORKSHOPS C.D. Graas, IBM
CONSULTANT R.C. Walker, SAR Associates
CONSULTANT D.F. Barber, Scien-Tech Associates

BOARD OF DIRECTORS

W.R. Tonti, Chair
IBM Microelectronics

A.N. Campbell
Sandia National Labs

N.R. Mielke
Intel

H.A. Schafft
NIST

L.A. Kasprzak
Consultant

B.M. Pietrucha
Rowan University

E.S. Synder
Sandia Technologies

J.W. McPherson
Texas Instruments

A.S. Oates
TSMC

A.G. Street
Integrated Reliability

PUBLISHED BY
THE ELECTRON DEVICE SOCIETY AND THE RELIABILITY SOCIETY
OF THE
INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limits of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved. Copyright © 2003 by the Institute of Electrical and Electronics Engineers, Inc.

IEEE Catalog No. 03CH37400
ISBN: 0-7803-7649-8 Softbound Edition
Library of Congress Number: 82-640313

PREFACE

The 41st IRPS proceedings is the culmination of 1000's of hours of author, committee and volunteer labor. It represents state-of-the-art in microelectronic reliability. In addition to a record number of submitted technical works, industry leaders from TSMC, Intel and Texas Instruments addressed the attendees. In keeping with the ever changing semiconductor industry, two keynote addresses were organized: one by Dr. Shang-yi Chiang, senior vice president and head of research and development group, of Taiwan Semiconductor Manufacturing Co., Ltd. (TSMC), "Technology and reliability challenges in the foundry business". And, one by Mark T. Bohr, an Intel Senior Fellow and director of process architecture and integration at Intel, "Technology and reliability challenges at integrated device manufacturers." At the Symposium Reception and Poster Session the speaker was Larry Hornbeck, Texas Instruments Fellow, Digital Light Processing, "The future of MEMS based projection display systems." Finally, a new "Reliability Year-in-Review" Seminar was added to the end of the IRPS.

The companion CDROM of the proceedings (IEEE Catalog No. 03CH37400C; ISBN: 0-7803-7650-1) contain many files where color is used and in some cases make viewing data graphs easier. Abstracts of the Sunday and Monday tutorials can be found in the last two pages of these proceedings.

A virtual IRPS 2003 on DVD-ROMs is available (www.irps.org) that provides video, audio, and presentation material for all the presentations.

TABLE OF CONTENTS

CIRCUITS 1

CHAIR: STEVE WALSTRA

Effect of gate oxide breakdown on RF device and circuit performance <i>H. Yang, J.S. Yuan, and E. Xiao</i>	1
On the degradation of P-MOSFETS in analog and RF circuit under inhomogeneous negative bias temperature stress <i>C. Schlünder, R. Brederlow, B. Ankele, A. Lill, K. Goser, and R. Thewes</i>	5
Modeling and experimental verification of the effect of gate oxide breakdown on CMOS inverters <i>R. Rodriguez, J.H. Stathis, and B.P. Linder</i>	11
Behavior of NBTI under AC dynamic circuit conditions <i>W. Abadeer and W. Ellis</i>	17

HIGH K DIELECTRICS 2A

CHAIRS: JAMES STATHIS AND MASAOKI NIWA

(Invited) Stress polarity dependence of degradation and breakdown of SiO ₂ /high-k stacks <i>R. Degraeve, T. Kauerauf, A. Kerber, E. Cartier, B. Govoreanu, P. Roussel, L. Pantisano, P. Blomme, B. Kaczer, and G. Groeseneken</i>	23
Accurate reliability evaluation of non-uniform ultrathin oxynitride and high-k layers <i>P. Roussel, R. Degraeve, A. Kerber, L. Pantisano, and G. Groeseneken</i>	29
Novel dielectric breakdown model of Hf-silicate with high temperature annealing <i>T. Yamaguchi, T. Ino, H. Satake, and N. Fukushima</i>	34
Characterization of the VT instability in SiO ₂ /HfO ₂ gate dielectrics <i>A. Kerber, E. Cartier, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H.E. Maes, and U. Schwalke</i>	41
Dynamic reliability characteristics of ultra-thin HfO ₂ <i>Y.H. Kim, K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Krishnan, A. Shahriar, and J.C. Lee</i>	46

SER ^{2/3}

CHAIRS: ROBERT BAUMAN AND PAUL DODD

(Invited) Neutron-induced latchup in SRAMs at ground level <i>P.E. Dodd, M.R. Shaneyfelt, J.R. Schwank, and G.L. Hash</i>	51
Measuring the width of transient pulses induced by ionising radiation <i>M. Nicolaidis and R. Perez</i>	56
A systematic approach to SER estimation and solutions <i>H.T. Nguyen and Y. Yagil</i>	60
Contribution of device simulation to SER understanding <i>J-M. Palau, M-C. Calvet, P.E. Dodd, F.W. Sexton, and P. Roche</i>	71

LATCH-UP ^{2/6}

CHAIRS: STEVEN VOLDMAN AND PATRICK JULIANO

(Invited) Latchup in CMOS <i>W.H. Morris</i>	76
A new I/O signal latchup phenomenon in voltage tolerance ESD protection circuits <i>J. Salcedo-Suner, R. Cline, C. Duvvury, A. Cadena-Hernandez, L. Ting, and J. Schichl</i>	85
New observance and analysis of various guard-ring structures on latch-up hardness by backside photo emission image <i>S. Liao, C. Niou, W.T.K. Chien, A. Guo, W. Dong, and C.Huang</i>	92
Transmission line pulse picosecond imaging circuit analysis methodology for evaluation of electrostatic discharge and latchup <i>A. Weger, S.H. Voldman, F. Stellari, P. Song, P. Sanda, and M. McManus</i>	99
A device level negative feedback in the emitter line of SCR-structures as a method to realize latch-up free ESD Protection <i>A. Concannon, V.A. Vashchenko, M. ter Beek, and P. Hopper</i>	105

LATE NEWS PAPERS ^{2/1}

CHAIRS: ANTONIETTE OLIVA AND VIJAY REDDY

A 90nm CMOS technology with modular quadruple gate oxides for advanced SoC applications <i>M.R. Mirabedini, V.P. Gopinath, A. Kamath, M.Y. Lee, W.J. Hsia, V. Hornback, Y. Le, A. Badowski, B. Baylis, E. Li, S. Prasad, O. Kobozeva, J. Haywood, W. Catabay, and W.C. Yeh</i>	112
Detailed Investigation of the Transient Local Tunneling in Gate Oxides <i>M.F. Beug, R. Ferretti, and K.R. Hofmann</i>	116
Abnormal Gate Oxide Thickening at Active Edge with SiN-Lined Shallow Trench Isolation <i>K.-S. Lee, J.-J. Han, S.-M. Shin, K.-H. Hwang, S.-W. Nam, H.-D. Lee, and C.-L. Song</i>	121
Using the Temperature Coefficient of the Resistance (TCR) as Early Reliability Indicator for Stressvoiding Risks in Copper Interconnects <i>A. von Glasow, A.H. Fischer, and G. Steinlesberger</i>	126
A study in flip-chip UBM/bump reliability with effects of Sn-Pb solder composition <i>J.D. Wu, P.J. Zheng, C.W. Lee, S.C. Hung, and J.J. Lee</i>	132

INTERCONNECTS ^{3/1}

CHAIRS: JAMES LLOYD AND JOSEPH CLEMENT

Line depletion electromigration characteristics of Cu interconnects <i>B. Li, T.D. Sullivan, and T.C. Lee</i>	140
The influence of the SiN-cap process on the electromigration and stressvoiding performance of dual damascene copper interconnects <i>A. von Glasow, A.H. Fischer, D. Bunel, G. Friese, A. Hausmann, O. Heitzsch, M. Hommel, J.Kriz, S. Penka, P. Raffin, C. Robin, H.-P. Sperlich, F. Ungar, and A.E. Zitzelsberger</i>	146
Electromigration improvement with CVD TiN(Si) barrier in copper dual damascene structures <i>G.B. Alers, A. Vijayendran, P. Gillespie, L. Chen, H. Cox, K. Lam, R. Augur, K. Shannon, K. Pfeifer, and M. Danek</i>	151
Stress-induced voiding and its geometry dependency characterization <i>K.Y.Y. Doong, R.C.J. Wang, S.C. Lin, L.J. Hung, S.Y. Lee, C.C. Chiu, D.H. Su, K.L. Young, K. Wu, and Y.K. Peng</i>	156

	On the use of highly accelerated electromigration tests (SWEAT) on copper <i>A.E. Zitzelsberger, R. Bauer, J. von Hagen, S. Penka, A. Pietsch, F. Ungar, and W. Walter</i>	161
--	---	-----

BEOL DIELECTRICS 3/3

CHAIRS: JAMES WALLS AND MIKE DION

51	Leakage, Breakdown, and TDDDB Characteristics of Porous Low-k Silica-Based Interconnect Dielectrics <i>E.T. Ogawa, J. Kim, G.S. Haase, H.C. Mogul, and J.W. McPherson</i>	166
56	The effect of low-K ILD on the electromigration reliability of Cu interconnects with different line lengths <i>C.S. Hau-Riege, A.P. Marathe, and V. Pham</i>	173

Transistors 3C

CHAIRS: MOHSEN ALAVI AND GIUSEPPE LAROSA

71	Evidence for hydrogen-related defects during NBTI stress in p-MOSFETs <i>V. Huard, F. Monsieur, G. Ribes, and S. Bruyere</i>	178
76	Negative bias temperature instability of pMOSFETs with ultra-thin SiON gate dielectrics <i>S. Tsujikawa, T. Mine, K. Watanabe, Y. Shimamoto, R. Tsuchiya, K. Ohnishi, T. Onai, J. Yugami, and S. Kimura</i>	183
85	Collapse of MOSFET drain current after soft breakdown and its dependence on the transistor aspect ratio W/L <i>A. Cester, S. Cimino, A. Paccagnella, G. Ghidini, and G. Guegan</i>	189
92	Dynamic NBTI of PMOS transistors and its Impact on MOSFET lifeline <i>G. Chen, K.Y. Chuah, M.F. Li, D.S.H. Chan, C.H. Ang, J.Z. Zheng, Y. Jin, and D.L. Kwong</i>	196
99	An improved interface characterization technique for a full-range profiling of oxide damage in ultra-thin gate oxide CMOS devices <i>S.-J. Chen, T.-C. Lin, D.-K. Lo, J.-J. Yang, S.S. Chung, T.-Y. Kao, R.-Y. Shiue, C.-J. Wang, and Y.-K. Peng</i>	203
105	Evaluation of the positive biased temperature stress stability in HfSiON gate dielectrics <i>A. Shanware, M.R. Visokay, J.J. Chambers, A.L.P. Rotondaro, H. Bu, M.J. Bevan, R. Khamankar, S. Aur, P.E. Nicollian, J.W. McPherson, and L. Colombo</i>	208
	Competing hot carrier degradation mechanisms in lateral n-type DMOS transistors <i>P. Moens, G. Van den bosch, and G. Groeseneken</i>	214

ESD 3D

CHAIRS: STEVE VOLDMAN AND PATRICK JULIANO

112	(Invited) ESD Challenges in Magnetic Recording: Past, Present and Future <i>A. Wallash</i>	222
116	Impact of scaling on the high current behavior of RF CMOS technology <i>G. Boselli, V. Reddy, and C. Duvvury</i>	229
121	Internal behavior of BCD ESD protection devices under very-fast TLP stress <i>M. Blaho, D. Pogany, E. Gornik, H. Wolf, H. Gieser, L. Zullino, E. Morena, R. Stella, and A. Andreini</i>	235
126	Moving current filaments in ESD protection devices and their relation to electrical characteristics <i>D. Pogany, S. Bychikhin, E. Gornik, M. Denison, N. Jensen, G. Groos, and M. Stecher</i>	241
132	Modeling of temperature dependent contact resistance for analysis of ESD reliability <i>K.-H. Oh, J.-H. Chun, K. Banerjee, C. Duvvury, and R.W. Dutton</i>	249
	Dynamic substrate resistance snapback triggering of ESD protection devices <i>V. Vassilev, G. Groeseneken, M. Steyaert, and H. Maes</i>	256
140	Increasing the ESD protection capability of over-voltage NMOS structures by comb-ballasting region design <i>V.A. Vashchenko, A. Concannon, M. ter Beek, and P. Hopper</i>	261
146	The failure mechanism of the high voltage tolerance IO buffer under ESD <i>J.-H. Lee, J.R. Shih, Y.H. Wu, and T.C. Ong</i>	269

BEOL DIELECTRICS

CHAIRS: JAMES WALLS AND MIKE DION

(Invited) Leakage Behavior and Reliability Assessment of Tantalum Oxide Dielectric MIM Capacitors <i>T. Rimmel, R. Ramprasad, and J. Walls</i>	277
A physical model of time-dependent dielectric breakdown in copper metallization <i>W. Wu, X. Duan, and J.S. Yuan</i>	282
Cu ion migration phenomena and its influence on TDDDB lifetime in Cu metallization <i>J. Noguchi, N. Miura, M. Kubo, T.I. Tamaru, H. Yamaguchi, N. Hamada, K. Makabe, R. Tsuneda, and K. Takeda</i>	287
Reliability and electric properties for PECVD a-SiNx:H films with an optical band-gap from 2.5 to 5.38eV <i>M.H.W.M. van Delden and P.J. van der Wel</i>	293

DEVICE & PROCESS

CHAIRS: VIJAY REDDY AND JEFF PETERSON

HSG storage capacitor dielectric reliability of 0.13 μm embedded DRAM CMOS technology <i>S. Bruyère, D. Roy, D. Jacques, and C. Boccaccio</i>	298
New process damage during the etching of small-contact on long floating conductor layer <i>J. Choi, D. Park, H. Moon, S. Lee, H. Ko, K. Yang, and W. Lee</i>	303
NMOS predope enhance off-state leakage current <i>K.Y. Lim, J. Lee, and E. Quek</i>	307
1/f noise degradation caused by Fowler-Nordheim tunneling stress in MOSFETs <i>M. Toita, S. Sugawa, A. Teramoto, T. Akaboshi, H. Imai, Asahi Kasei and T. Ohmi</i>	313

COMPOUND SEMICONDUCTORS

CHAIRS: PETER ERSLAND AND FRANK GAO

(Invited) Semiconductor Reliability Challenges from the Fabless Company Perspective <i>T.M. Kole</i>	318
Current collapse induced in AlGaIn/GaN HEMTs by short-term DC bias stress <i>J.A. Mittereder, S.C. Binari, P.B. Klein, J.A. Roussos, D.S. Katzer, D.F. Storm, D.D. Koleske, A.E. Wickenden, and R.L. Henry</i>	320
Bias acceleration model of drain resistance degradation in InP-based HEMTs <i>Y.K. Fukai, S. Sugitani, T. Enoki, H. Kitabayashi, T. Makimura, Y. Yamane, and M. Muraguchi</i>	324
Reliability characteristics of p-HEMT resulting from electron interaction with interface states under the gate <i>S. Mil'shtein, P. Ersland, C. Gil, and S. Somisetty</i>	329

SiGe

CHAIRS: PETER ERSLAND AND FRANK GAO

(Invited) SiGe HBT Performance and Reliability Trends through fT of 350GHz <i>G. Freeman, J.-S. Rieh, B. Jagannathan, Z. Yang, F. Guarin, A. Joseph, and D. Ahlgren</i>	332
Avalanche current induced hot carrier degradation in 200GHz SiGe heterojunction bipolar transistors <i>Z. Yang, F. Guarin, E. Hostetter, and G. Freeman</i>	339
Characterization of light emission from SiGe heterojunction bipolar transistor for photon emission microscopy applications <i>S. Polonsky, A. Talalaevskii, and M. McManus</i>	344
The influence of process and design of subcollectors on the ESD robustness of ESD structures and silicon germanium heterojunction bipolar transistors in a BiCMOS SiGe Technology <i>S.H. Voldman, L. Lanzerotti, B. Ronan, S. St.Onge, and J. Dunn</i>	347
Investigation of ESD devices in 0.18- μm SiGe BiCMOS process <i>S.-S. Chen, T.-Y. Chen, T.-H. Tang, T.-L. Hsu, H.-C. Tseng, J.-K. Chen, and C.-H. Chou</i>	357

PRODUCT RELIABILITY

CHAIRS: CAROLE GRAAS AND NICK LYCOUDES

DRAM reliability characterization by using dynamic operation stress in wafer burn-In mode <i>I.-G. Kim, S.-K. Choi, J.-H. Choi, and J.-S. Park</i>	361
---	-----

	Challenges of testing high-volume, low-cost 8-bit microcontrollers <i>M. Stout, K. Tumin, C. Vargas, and B. Gotchall</i>	366
..... 277	Correlation of the VT drift in a-Si:H TFT to the optically observed flicker increase in AMLCD <i>C.-C. Huang, J.H. Constable, B. Yost, and R.G. Greene</i>	372
..... 282	Reliability qualification of a smart power technology for high temperature application based on physics-of-failure and risk & opportunity assessment <i>A. Preussger, W. Kanert, and W. Gerling</i>	378
..... 287	Product level verification of gate oxide reliability projections using DRAM chips <i>R.-P. Vollertsen, K. Nierle, E.Y. Wu, and S. Wen</i>	385
..... 293	Investigation of wafer level burn-In to SoC memory: 1TRAM <i>Y.L. Pan, S.H. Chen, C.H. Lu, and J.J. Wang</i>	391
	Practical WLRC methodology & applications in a wafer foundry <i>W.T.K. Chien, S. Chiang, S. Tseng, C.H.J. Huang, K. Yang, W. Wang, and J. Zhou</i>	395
..... 298	GATE DIELECTRICS 512 CHAIRS: JAMES STATHIS AND MASAOKI NIWA	
..... 303	Growth and scaling of oxide conduction after breakdown <i>B.P. Linder, J.H. Stathis, D.J. Frank, S. Lombardo, and A. Vayshenker</i>	402
..... 307	A phenomenological theory of correlated multiple soft-breakdown events in ultra-thin gate dielectrics <i>M.A. Alam and R.K. Smith</i>	406
..... 313	Analysis of quantum yield in n-channel MOSFETs <i>A.S. Spinelli, D. Ielmini, A.L. Lacaita, A. Sebastiani, and G. Ghidini</i>	412
	Temperature dependence and conduction mechanism after analog soft breakdown <i>T. Nigam, S. Martin, and D. Abusch-Magder</i>	417
..... 318	Evidence for defect-generation-driven wear-out of breakdown conduction path in ultra thin oxides <i>F. Monsieur, E. Vincent, G. Ribes, V. Huard, S. Bruyère, D. Roy, G. Pananakakis, and G. Ghibaudo</i>	424
320	Soft breakdown in thin gate oxide – a measurement artifact <i>K.P. Cheung</i>	432
324	Negative substrate bias enhanced breakdown hardness in ultra-thin oxide pMOSFETs <i>T. Wang, C.W. Tsai, M.C. Chen, C.T. Chan, H.K. Chiang, S.H. Lu, H.C. Hu, T.F. Chen, C.K. Yang, M.T. Lee, D.Y. Wu, J.K. Chen, S.C. Chien, and S.W. Sun</i>	437
329	PACKAGING 53 CHAIRS: MICHELLE RASCO AND SIDHARTH	
	(Invited) Wheatstone Bridge Method for Electromigration Study of Solder Balls in Flip-Chip Packages <i>M. Ding, H. Matsushashi, P.S. Ho, A. Marathe, R.N. Master, and V. Pham</i>	442
32	Board level solder reliability vs ramp rate & dwell time during temperature cycling <i>C. Zhai, Sidharth, and R.C. Blish</i>	447
39	A simple model for the mode II popcorn effect in thin plastic IC packages <i>P. Alpern and K.C. Lee</i>	452
44	Advanced getter solutions at wafer level to assure high reliability to the last generations MEMs <i>M. Moraja, M. Amiotti, and R.C. Kullberg</i>	458
	MEMS 50 CHAIRS: DANELLE TANNER AND MICHAEL DOUGLASS	
7	(Invited) Instrumentation for Genome Analysis (and beyond) based on the TI Digital Micromirror Device <i>H.R. Garner</i>	460
7	Effect of Al ₂ O ₃ ALD Nanocoatings on the thermo-mechanical behavior of Au/Si MEMS structures <i>K. Gall, M.L. Dunn, M. Hulse, D. Finch, and S.M. George</i>	463
	Effects of operating conditions on DMD hinge memory lifetime <i>A.B. Sontheimer and D.J. Mehrl</i>	473
	Reliability of MEMS-based mass-flow controllers for semiconductor processing <i>E. Lawrence and A.K. Henning</i>	478

On-chip monitoring of MEMS gear motion <i>D.M. Tanner, S.E. Swanson, J. A. Walraven, and J.L. Dohner</i>	484
---	-----

MEMORY

CHAIRS: DOMOKOS HADNAGY AND GUOQIAO TAO

Variable stress-induced leakage current and analysis of anomalous charge loss for Flash memory application <i>R. Yamada and T.-J. King</i>	491
Degradation of tunnel oxide by FN current stress and Its effects on data retention characteristics of 90-nm NAND Flash memory cells <i>J.-D. Lee, J.-H. Choi, D. Park, and K. Kim</i>	497
Data retention, endurance and acceleration factors of NROM devices <i>M. Janai</i>	502
Study of data retention for nanocrystal Flash memories <i>C.M. Compagnoni, D. Ielmini, A.S. Spinelli, A.L. Lacaita, C. Previtati, and C. Gerardi</i>	506
An enhanced erase mechanism in Flash memory and Its implication on endurance reliability <i>J.M.Z. Tseng, B.J. Larsen, Y. Xiao, J. Yount, T. Randazzo, S. Shore, G. Miller, and D.A. Erickson</i>	513
Effect of programming biases on the reliability of CHE and CHISEL Flash EEPROMs <i>N.R. Mohapatra, S. Mahapatra, V.R. Rao, S. Shukuri, and J. Bude</i>	518

FAILURE ANALYSIS

CHAIRS: DAVID H. SU AND SCOTT WILLS

(Invited ESREF) Lifetime prediction and design of reliability tests for high-power devices in automotive applications <i>M. Ciappa, F. Carbognani, P. Cova, and W. Fichtener</i>	523
High resolution backside fault isolation technique by directly forming Si substrate into solid immersion lens <i>T. Koyama, E. Yoshida, J. Komori, Y. Mashiko, T. Nakasuji, and H. Katoh</i>	529
Reliability issues and advanced failure analysis deprocessing techniques for copper/low-k technology <i>H. Wu, J. Cargo, C. Peridier, and J. Serpiello</i>	536
Automated PICA transistor channeling and spatial-temporal photon correlation for faster IC diagnosis <i>R. Desplats, F. Beaudoin, G. Faggion, O. Jesson, P. Perdu, M. Leibowitz, T. Lundquist, and K. Shaht</i>	545
Laser interaction with SiCr thin film resistors – the bubble theory <i>E. Coyne</i>	553
A new approach to detect small-sized oxygen precipitates in Si wafers using reactive ion etching <i>K. Nakashima, T. Yoshida, Y. Watanabe, and Y. Mitsushima</i>	559
Consistency of optical data from PICA <i>T. Lundquist, K. Shah, A. Abraham, and W. Ng</i>	564

CIRCUITS POSTERS

A method to comprehend the impact of interconnect coupling effects on gate oxide reliability <i>A.A. Mutlu and P. Aminzadeh</i>	570
ARET for system-level IC reliability simulation <i>X. Xuan, A. Chatterjee, and A.D. Singh</i>	572

COMPOUND SEMICONDUCTORS POSTERS

Drain avalanche breakdown and gate instabilities in 4H-SiC MESFET's <i>H. Lv, Y. Zhang, and Y. Zhang</i>	574
A study on GaAs FET's failure mechanism and experimental technology of rapid evaluation of reliability <i>L. Zhiguo, S. Zengchao, S. Dapeng, C. Yaohai, Z. Zhongrong, and Z. Wanrong</i>	576

DEVICE DIELECTRICS POSTERS

A proper lifetime-prediction method of pMOSFET with 1.1nm gate dielectrics in the lower testing voltage region <i>N. Tamura and M. Kase</i>	578
Experimental study and modeling of the temperature dependence of soft breakdown conduction in ultrathin gate oxides <i>A. Avellan, E. Miranda, B. Sell, and W. Krautschneider</i>	579
Voltage-driven distribution of gate oxide breakdown <i>A. Hiraiwa, S. Sakai, and D. Ishikawa</i>	582

DEVICE & PROCESS POSTERS

484	DBIE shape and hardness dependence on gate oxide breakdown location in MOSFET channel <i>K.L. Pey, C.H. Tung, M.K. Radhakrishnan, L.J. Tang, and W.H. Lin</i>	584
	Defect passivation and dark count in Geiger-mode avalanche photodiodes <i>J.C. Jackson, G. Healy, A-M. Kelleher, J. Alderman, J. Donnelly, P.K. Hurley, A.P. Morrison, and A. Mathewson</i>	586

FAILURE ANALYSIS POSTERS

491	Localization and analysis of functional failures in deep submicron advanced ASIC products <i>M. Rubin</i>	588
497	FIB-induced deposition of conducting material with intermediate resistivity material for design debugging <i>G.Y. Gu, N.J. Bassom, J.D. Casey, Jr., L. Scipioni, A. Saxonis, and C. Huynh</i>	590

HIGH K DIELECTRICS POSTER

502	Temperature dependent current and charge trapping in thick SiO ₂ /ZrO ₂ stacks <i>P. Blomme, B. Govoreanu, J. Van Houdt, and K. De Meyer</i>	592
-----	---	-----

INTERCONNECTS POSTERS

513	Effect of current distribution on the reliability of multi-terminal Cu dual-damascene interconnect trees <i>C.L. Gan, C.V. Thompson, K.L. Pey, W.K. Choi, C.W. Chang, and Q. Guo</i>	594
518	Real case studies of failure mechanisms for Cu trench electromigration <i>J.B. Lai, J.L. Yang, H.W. Yang, R.L. Hwang, D. Su, H. Chuang, and Y.S. Huang</i>	596

BEOL DIELECTRICS POSTER

523	TDDDB and voltage-ramp reliability of SiC-based dielectric diffusion barriers in Cu/Low-k interconnects <i>K. Jow, G. Alers, M. Sanganeria, G. Harm, H. Fu, X. Tang, G. Kooi, G. Ray, and M. Danek</i>	598
-----	---	-----

PRODUCT RELIABILITY POSTERS

529	Defect based testing with new ISB current strategy <i>B. Lisenker</i>	600
536	Wafer level reliability monitoring strategy of an advanced multi-process CMOS foundry <i>A. Scarpa and G. Tao</i>	602
545	Process qualification strategy for advanced embedded non-volatile memory technology — The Philips' 0.18 μm embedded flash case <i>G. Tao, A. Scarpa, K. van Dijk, and F.G. Kuper</i>	604

TRANSISTORS POSTERS

559	Transient effects and characterization methodology of negative bias temperature instability in pMOS transistors <i>M. Ershov, R. Lindley, S. Saxena, A. Shibkov, S. Minehane, J. Babcock, S. Winters, H. Karbasi, T. Yamashita, P. Clifton, and M. Redford</i>	606
564	Design optimization of N-LDMOS transistor arrays for hot carrier lifetime enhancement <i>D.J. Brisbin, A. Strachan, and P. Chaparala</i>	608
570	Time and voltage dependence of degradation and recovery under pulsed negative bias temperature stress <i>H. Usui, M. Kanno, and T. Morikawa</i>	610
72	The study of compressive and tensile stress on MOSFET's I-V, C-V characteristics and It's impacts on hot carrier injection and negative bias Temperature Instability <i>J.R. Shih, J.J. Wang, Y.M. Lin, Ken Wu, Y. Peng, and J.T. Yue</i>	612
74	Biographies.....	614
	Page Number Cross-reference to Session/Poster Paper #.....	638
76	2003 Committees.....	639
	2001 Paper Awards.....	643
8	2003 Tutorial Program Abstracts.....	644