



IEEE



2002

IEEE

International

Reliability

Physics

Symposium

Proceedings

40th Annual

Dallas, Texas • April 7–11, 2002

**Sponsored by
the IEEE Electron Devices Society and
the IEEE Reliability Society**

IEEE Catalog No. 02CH37320

2002 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

SYMPOSIUM OFFICERS

GENERAL CHAIR W.R. Tonti, *IBM Microelectronics*
VICE GENERAL CHAIR E.S. Snyder, *Sandia Technologies*
SECRETARY J.F. Conley, Jr., *Sharp Labs of American*
FINANCE C.D. Graas, *Infineon Technologies*

SYMPOSIUM COMMITTEE CHAIRS

TECHNICAL PROGRAM B.M. Pietrucha, *Rowan University*
PUBLICITY W.W. Abadeer, *IBM Microelectronics*
REGISTRATION E.I. Cole, Jr., *Sandia National Labs*
ARRANGEMENTS T.A. Rost, *Texas Instruments*
AUDIO-VISUAL J.S. Suehle, *NIST*
PUBLICATIONS R.C. Lacoé, *The Aerospace Corporation*
EQUIPMENT DEMOS D.L. Barton, *Sandia National Labs*
TUTORIAL T.M. Moore, *Omniprobe*
WORKSHOPS S. Krishnan, *Texas Instruments*
CONSULTANT R.C. Walker, *SAR Associates*
CONSULTANT D.F. Barber, *Scien-Tech Associates*

BOARD OF DIRECTORS

A.S. Oates
Agere Systems

A.N. Campbell
Sandia National Labs

H.A. Schafft
NIST

L.A. Kasprzak
Consultant

E.S. Synder
Sandia Technologies

J.E. Klema
Motorola

A.G. Street
Integrated Reliability

N.R. Mielke
Intel

W.R. Tonti
IBM Microelectronics

PUBLISHED BY
THE ELECTRON DEVICE SOCIETY AND THE RELIABILITY SOCIETY
OF THE
INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limits of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331. All rights reserved. Copyright © 2002 by the Institute of Electrical and Electronics Engineers, Inc.

IEEE Catalog No. 02CH37320
ISBN: 0-7803-7352-9 Softbound Edition
Library of Congress Number: 82-640313

TABLE OF CONTENTS

NON VOLATILE MEMORIES

Session Co-Chairs: Neal R. Mielke and Fred G. Kuper

Localization of SILC in Flash Memories after Program/Erase Cycling <i>D. Ielmini, A.S. Spinelli, A.L. Lacaita, R. Leone, and A. Visconti</i>	1
A New Reliability Model for Post-Cycling Charge Retention of Flash Memories <i>H.P. Belgal, N. Righos, I. Kalastirsky, J.J. Peterson, R. Shiner, and N.R. Mielke</i>	7
Statistical Modeling of the Program/Erase Cycling Acceleration of Low Temperature Data Retention in Floating Gate Nonvolatile Memories <i>A. Hoefer, JM.. Higman, T.S. Harp, and P.J. Kuhn</i>	21
Physical Description of Anomalous Charge Loss of Floating Gate Based NVM's and Identification of its Dominant Parameter <i>F. Schuler, R. Degraeve, P. Hendrickx, and D. Wellekens</i>	26
Cause of Data Retention Loss in a Nitride-Based Localized Trapping Storage Flash Memory Cell <i>W.J. Tsai, S.H. Gu, N.K. Zous, C.C. Yeh, C.C. Liu, C.H. Chen, T. Wang, S. Pan, and C.Y. Lu</i>	34
Empirical Model for Fatigue of PZT Ferroelectric Memories <i>J. Rodriguez, J.W. McPherson, T. Moise, S. Summerfelt, S. Aggarwal, K.R. Udayakumar, S. Gilbert and C. Dunn</i>	39

DIELECTRICS I

Session Co-Chairs: Eric M. Vogel and M. Ashraful Alam

A Thorough Investigation of Progressive Breakdown in Ultra-thin Oxides: Physical Understanding and Application for Industrial Reliability Assessment <i>F. Monsieur, E. Vincent, D. Roy, S. Bruyere, G. Pananakakis, and G. Ghibaudo</i>	45
Location and Hardness of the Oxide Breakdown in Short Channel n- and p-MOSFETs <i>F. Crupi, B. Kaczer, R. Degraeve, A. De Keersgieter, and G. Groeseneken</i>	55
Polarity-Dependent Oxide Breakdown of NFET Devices for Ultra-Thin Gate Oxide <i>E. Wu, W. Lai, M. Khare, J. Suñé, L.K. Han, J. McKenna, R. Bolman, D. Harmon, and A. Strong</i>	60
Gate Oxide Reliability Of Drain-Side Stresses Compared To Gate Stresses <i>N.A. Dumin, K. Liu, and S.-H. Yang</i>	73

HOT CARRIERS

Session Co-Chairs: Giuseppe La Rosa and Janet Wang-Ratkovic

NBT-induced Hot Carrier (HC) Effect: Positive Feedback Mechanism in p-MOSFET's Degradation <i>H. Aono, E. Murakami, K. Okuyama, K. Makabe, K. Kuroda, K. Watanabe, H. Ozaki, K. Yanagisawa, K. Kubota, and Y. Ohji</i>	79
A Drain Avalanche Hot Carrier Lifetime Model for n- and p-Channel MOSFET's <i>N. Koike and K. Tatsuuma</i>	86
Excess Hot-Carrier Currents in SOI MOSFETs and Its Implications <i>P. Su, K. Goto, T. Sugii, and C. Hu</i>	93
Effects of Hot-Carrier Stress on the RF Performance of 0.18 μm Technology NMOSFETs and Circuits <i>S. Naseh, M.J. Deen, and O. Marinov</i>	98
Hot Carrier Reliability of N-LDMOS Transistor Arrays for Power BiCMOS Applications <i>D.J. Brisbin, A. Strachan, and P. Chaparala</i>	105

MEMS

Session Co-Chairs: Danelle M. Tanner and Michael R. Douglass

Invited Paper: RF MEMS Switches and Applications <i>H.S. Newman</i>	111
Invited Paper: Techniques for Reliability Analysis of MEMS RF Switch <i>J. DeNatale, R. Mihailovich, and J. Waldrop</i>	116

Digital Micromirror Device (DMD) Hinge Memory Lifetime Reliability Modeling <i>A.B. Sontheimer</i>	118
---	-----

Pin-Joint Design Effect on the Reliability of a Polysilicon Microengine <i>D.M. Tanner, J.A. Walraven, S.S. Mani, and S.E. Swanson</i>	122
---	-----

ASSEMBLY/PACKAGING

Session Co-Chairs: Thomas M. Moore and Sidharth Sidharth

Invited Paper: Product-specific ‘Moisture Levels’: A Conceptual Framework <i>R.C. Blish, II and S. Sidharth</i>	130
--	-----

Invited Paper: Hermeticity and Stiction in MEMS Packaging <i>S.J. Jacobs, S.A. Miller, J.J. Malone, W.C. McDonald, V.C. Lopes, and L.K. Magel</i>	136
--	-----

Invited Paper: Probing and Wire Bonding of Aluminum Capped Copper Pads <i>G. Hotchkiss, J. Aronoff, J. Broz, C. Hartfield, R. James, L. Stark, W. Subido, V. Sundararaman, and H. Test</i>	140
---	-----

Accelerated Reliability - Thermal And Mechanical Fatigue Solder Joint Methodologies <i>N.E. Strifas, C. Vaughan, and M. Ruzzene</i>	144
--	-----

ESD & LATCHUP

Session Co-Chairs: Jeremy C. Smith and Stephen G. Beebe

Investigation of Gate to Contact Spacing Effect on ESD Robustness of Salicided Deep Submicron Single Finger NMOS Transistors <i>K.-H. Oh, C. Duvvury, K. Banerjee, and R.W. Dutton</i>	148
---	-----

Novel ESD Protection Structure with Embedded SCR LDMOS for Smart Power Technology <i>J.H. Lee, J.R. Shih, C.S. Tang, K.C. Liu, Y.H. Wu, R.Y. Shiue, T.C. Ong, Y.K. Peng, and J.T. Yue</i>	156
--	-----

ESD Circuit Simulation for the Prevention of ESD Failures — Application to Products in a 0.18 μm CMOS Technology <i>H. Wolf, H. Gieser, W. Stadler, and K. Esmark</i>	162
--	-----

Electrostatic Discharge Induced Oxide Breakdown Characterization in a 0.1 μm CMOS Technology <i>A. Salman, R. Gauthier, E. Wu, P. Riess, C. Putnam, M. Muhammad, M. Woo, and D. Ioannou</i>	170
--	-----

COMPOUND SEMICONDUCTORS I

Session Co-Chairs: Wallace T. Anderson and Anthony Immorlica

High Current Transmission Line Pulse (TLP) and ESD Characterization of a Silicon Germanium Heterojunction Bipolar Transistor with Carbon Incorporated <i>B. Ronan, S.H. Voldman, L.D. Lanzerotti, J. Rascoe, D. Sheridan, and K. Rajendran</i> ,	175
---	-----

Wafer Level Forward Current Reliability Analysis of 120GHz Production SiGe HBTs under Accelerated Current Stress <i>J.-S. Rieh, K. Watson, F. Guarin, Z. Yang, P.-C. Wang, A. Joseph, G. Freeman, and S. Subbanna</i>	184
--	-----

Physical Mechanisms of Performance Instabilities such as Gate-Lag and Kink Phenomena in GaAs MESFETs <i>Y. Mitani, A. Wakabayashi, and K. Horio</i>	189
--	-----

FAILURE ANALYSIS

Session Co-Chairs: Travis M. Eiles and Michael R. Bruce

Recovery of Shifted MOS Parameters Induced by Focused Ion Beam Exposure <i>K. Chen, , T. Chatterjee, J. Parker, T. Henderson, R.S. Martin, and H. Edwards</i>	194
--	-----

Reliability of Ultra Thinning of Flip Chips for Through-Silicon Analyses <i>C.-C. Tsao, E. Le Roy, S. Saha, L. Ansorge, and M.E. Potter</i>	198
--	-----

Neural Network Classification of Photoemission Spectra <i>S.J. Frank</i>	205
---	-----

Physical Analysis of Ti-migration in 33Å Gate Oxide Breakdown <i>K.L. Pey, C.H. Tung, W.H. Lin, and M.K. Radhakrishnan</i>	210
---	-----

PRODUCT RELIABILITY I

Session Co-Chairs: Robert V. Knoell and Walter C. Riordan

Soft Error Rate Mitigation Techniques for Modern Microcircuits <i>D.G. Mavis and P.H. Eaton</i>	216
--	-----

SER Reliability of 1TRAM Designs <i>D. Sinitsky, S. Peng, J. Wang, T.C. Ong, E. Chen, and F.C. Hsu,</i>	226
--	-----

COMPOUND SEMICONDUCTORS II

Session Co-Chairs: Wallace T. Anderson and Anthony Immorlica

Reliability Test of MESFETs in Presence of Hot Electrons <i>S. Mil'shtein, P. Ersland, and C. Gil</i>	230
Innovative Nitride Passivation on Pseudomorphic GaAs HEMTs and Its Impact on Device Performance <i>Y.-C. Chou, P. Nam, , G.P. Li, R. Lai, H.K. Kim, R. Grundbacher, E. Ahlers, Y. Ra, Q. Xu, Y. Ra, M. Biedenbender, and A. Oki</i>	235
Evolution of DC and RF Degradation Induced by High-Temperature Accelerated Lifetest of Pseudomorphic GaAs and InGaAs/InAlAs/InP HEMT MMICs <i>Y.-C. Chou, D. Leung, R. Lai, R. Grundbacher, D. Eng, J.R. Scarpulla, M. Barsky, P.H. Liu, M. Biedenbender, A. Oki, and D. Streit</i>	241

DEVICE & PROCESS

Session Co-Chairs: Prasad Chaparala and Srikanth Krishnan

Impact of Negative Bias Temperature Instability on Digital Circuit Reliability <i>V.K. Reddy, A.T. Krishnan, A. Marshall, J. Rodriguez, S. Natarajan, T.A. Rost, and S. Krishnan</i>	248
Leakage Current and Reliability Evaluation of Ultra-thin Reoxidized Nitride and Comparison with Silicon Dioxides <i>E.Y. Wu, R.-P. Vollertsen, R. Jammy, A. Strong, and C. Radens</i>	255
Extending the Reliability Scaling Limit of Gate Dielectrics through Remote Plasma Nitridation of N ₂ -O-Grown Oxides and NO RTA Treatment <i>C.H. Liu, H.-S. Lin, Y.Y. Lin, M.G. Chen, T.M. Pan, C.J. Kao, K.T. Huang, S.H. Lin, Y.C. Sheng, W.T. Chang, J.H. Lee, M. Huang, C.S. Hsiung, S. Huang-Lu, C.C. Hsu, A.Y. Liang, J.Chen, W.Y. Hsieh, P.W. Yen, S.C. Chien, Y.T. Loh, Y.J. Chang, and F.-T. Liou</i>	268
N-FET HCI Reliability Improvement by Nitrogen Interstitialization and its Mechanism <i>J.R. Shih, M.C. Chiang, H.C. Lin, R.Y. Shiue, Y.K. Peng, and J.T. Yue</i>	272
Mechanism of Device Degradation under AC stress in Low-Temperature Polycrystalline Silicon TFTs <i>Y. Toyota, T. Shiba, and M. Ohkura</i>	278

PRODUCT RELIABILITY II

Session Co-Chairs: Robert V. Knoell and Walter C. Riordan

Evaluation of STI Degradation Causing DRAM Standby Current Failure in Burn-in Mode Operation Using a Carrier Injection Method <i>S.W. Hong, G.Y. Jin, H.W. Seo, D.I. Lee, J.H. Song, J.Y. Noh, Y.C. Oh, J.Y. Kim, D.H. Kim, H.H. Kim, D.J. Won, W.W. Lee, D.H. Song, K.Y. Lee, and W.-S. Lee</i>	283
Charge Trapping Induced DRAM Data Retention Time Degradation under Wafer-Level Burn-in Stress <i>H.W. Seo, G.-Y. Jin, K.-H. Yang, Y.-J. Lee, J.-H. Lee, D.-H. Song, Y.-C. Oh, J.-Y. Noh, S.-W. Hong, D.-H. Kim, J.-Y. Kim, H.-H. Kim, D.-J. Won, and W.-S. Lee</i>	287
A Technique to Predict Gate Oxide Reliability Using Fast On-Line Ramped Q _{BD} Testing <i>E. Mullen, C. Leveugle, J. Molyneaux, J. Prendergast, and J.S. Suehle</i>	292

INTERCONNECTS

Session Co-Chairs: Michael Dion and James A. Walls

Invited Paper: Investigation of Via-Dominated Multi-Modal Electromigration Failure Distributions in Dual Damascene Cu Interconnects With a Discussion of the Statistical Implications <i>J.P. Gill, T.D. Sullivan, S. Yankee, H. Barth, and A. von Glasow</i>	298
Pseudo-Breakdown Events Induced by Biased-Thermal-Stressing of Intra-Level Cu Interconnects-Reliability & Performance Impact <i>W.S. Song, T.J. Kim, D.H. Lee, T.K. Kim, C.S. Lee, J.W. Kim, S.Y. Kim, D.K. Jeong, K.C. Park, Y.J. Wee, B.S. Suh, S.M. Choi, H.-K. Kang, K.P. Suh, J.T. Moon, and S.U. Kim</i>	305
Stress-Induced Voiding Under Vias Connected To Wide Cu Metal Leads <i>E.T. Ogawa, J.W. McPherson, J.A. Rosal, K.J. Dickerson, T.-C. Chiu, L.Y. Tsung, M.K. Jain, T.D. Bonifield, J.C. Ondrussek, and W.R. McKee</i>	312

Electromigration Study of Cu/low k Dual-damascene Interconnects <i>K.-D. Lee, X. Lu, E.T. Ogawa, H. Matsuhashi, V.A. Blaschke, R. Augur, and P.S. Ho</i>	322
Electromigration of Al and Cu Metallization Using WLR Isothermal Method <i>T.C. Lee, M. Ruprecht, D.M. Tibel, T.D. Sullivan, and S. Wen</i>	327
Modeling and Analysis of Via Hot Spots and Implications for ULSI Interconnect Reliability <i>S. Im, K. Banerjee, and K.E. Goodson</i>	336

PROCESS INDUCED DAMAGE

Session Co-Chairs: Tomasz Brozek and Kin P. Cheung

Invited Paper: Use of EEPROM-based Sensors in Investigating Physical Mechanisms Responsible for Charging Damage <i>W. Lukaszek</i>	346
Influence of Plasma Edge Damage on Erase Characteristics of NOR Flash EEPROM using Channel Erase Method <i>D.-K. Lee, W.H. Lee, Y.-H. Na, K.-S. Kim, K.-O. Ahn, K.-D. Suh, and Y. Roh</i>	354
Enhanced Plasma Charging Damage due to AC Charging Effect <i>Y. Jin, W.Y. Teo, Y.T. Hou, F.H. Gn, H.F. Lim, Z.Y. Han, and M.F. Li</i>	359
The Influence of IMD Bake Process on Buried Channel PMOS Hot Carrier Reliability of Advanced DRAM <i>S.J. Ahn, J.K. Lee, G.T. Jung, C.H. Cho, Y.S. Hwang, D.W. Shin, H.S. Jeong, and K. Kim</i>	365
Impact of Focused Ion Beam Assisted Front End Processing on n-MOSFET Degradation <i>A. Lugstein, W. Brezna, and E. Bertagnolli</i>	369

SPECIAL TOPIC: GERMICIDAL IRRADIATION OF THE US MAIL: CAN ICs SURVIVE WHILE BACTERIA PERISH?

Session Chair: Bernard Pietrucha

The Effects of Total Ionizing Dose Irradiation on CMOS Technology and the use of Design Techniques to Mitigate Total Dose Effects (abstract) <i>R.C. Lacoé</i>	376
Effects of E-Beam Mail Sanitizing Process on Commercial Electronics (abstract) <i>F.W. Sexton, P.E. Dodd, M.R. Shaneyfelt, and J.R. Schwank</i>	376
Filter Optimization for X-Ray Inspection of Surface-Mounted ICs <i>R.C. Blish, II, S.X. Li, and D. Lehtonen</i>	377

DIELECTRICS II

Session Co-Chairs: Eric M. Vogel and M. Ashraful Alam

Imaging Breakdown Spots in SiO ₂ Films and MOS Devices with a Conductive Atomic Force Microscope <i>M. Porti, M.C. Blüm, M. Nafria, and X. Aymerich</i>	380
Analysis of Exponential Decay Transient Current in MOS Capacitors <i>R. Yamada and J. Yugami</i>	387
Modeling of Substrate Related Extrinsic Oxide Failure Distributions <i>T. Pompl, M. Kerber, G. Innertsberger, K.-H. Allers, M. Obry, A. Krasemann, and D. Temmler</i>	393
Soft Breakdown Enhanced Hysteresis Effects in Ultra-Thin Oxide SOI nMOSFETs <i>M.C. Chen, C.W. Tsai, S.H. Gu, T. Wang, S.H. Lu, S.W. Lin, G.S. Yang, J.K. Chen, S.C. Chien, Y.T. Loh, and F.T. Liu</i>	404
Time-dependent Dielectric Breakdown in Poly-Si CVD HfO ₂ Gate Stack <i>S.-J. Lee, C.H. Lee, C.H. Choi, and D.L. Kwong</i>	409

DEVICE DIELECTRICS POSTERS

Stress Induced Leakage Current and Bulk Oxide Trapping: Temperature Evolution <i>G. Ghidini, A. Sebastiani, and D. Brazzelli</i>	415
Atomistic Model For E' Center Generation During Electrical Stress <i>G. Bersuker, A. Korkin, Y. Jeon, and H.R. Huff</i>	417
Charging Effects on Reliability of HfO_2 Devices with Polysilicon Gate Electrode <i>K. Onishi, C. S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee</i>	419
Modeling Kinetics of Gate Oxide Reliability Using Stretched Exponents <i>M.S. Krishnan and V. Kol'dyaev</i>	421

DEVICE & PROCESS POSTERS

Electrothermal Simulation of SiC GTO Thyristor Containing Gate and Drift Regions of the Same or Opposite Polarity in a Clamped Inductive Load Circuit <i>P.B. Shah</i>	423
Temperature Dependence of $R_{\text{on,sp}}$ in Silicon Carbide and GaAs Schottky Diode <i>J. Luo, K.J. Chung, H. Huang, and J.B. Bernstein</i>	425

HOT CARRIERS POSTERS

Sub-0.25 μm MOSFET Impact Ionization and Photon Generation Dynamics Based on High-resolution Photo-Emission Spectrum Analysis <i>R. Muniandy</i>	427
Hot Carrier Reliability of n-MOSFET with Ultra-thin HfO_2 Gate Dielectric and Poly-Si Gate <i>Q. Lu, H. Takeuchi, R. Lin, T.-J. King, C. Hu, K. Onishi, R. Choi, C.-S. Kang, and J.C. Lee</i>	429

INTERCONNECTS POSTERS

Electrical Characterization of Copper Penetration Effects in Silicon Dioxide <i>J. Cluzel, F. Mondon, D. Blachier, Y. Morand, L. Martel, and G. Reimbold</i> ,	431
Electromigration Threshold Length Effect in Dual Damascene Copper-Oxide Interconnects <i>L. Arnaud</i>	433
Recovery of Open Via after Electromigration in Cu Dual Damascene Interconnect <i>Y. Sun, P. Zhou, D.-Y. Kim, K.E. Goodson, and S.S. Wong</i>	435

NON VOLATILE MEMORIES POSTERS

A Complete Study of SILC Effects on E ² PROM Reliability <i>L.Larcher, S. Bertulu, and P. Pavan</i>	437
Effects of Fowler Nordheim Tunneling Stress vs. Channel Hot Electron Stress on Data Retention Characteristics of Floating Gate Non-Volatile Memories <i>M.Suhail, T.Harp, J. Bridwell, and P.J. Kuhn</i>	439
Biographies	441
Page Number Cross-reference to Session/Poster Paper #	465
2002 Committees	466
2000 Paper Awards	470
2002 Tutorial Program Abstracts	473