

Andreas Martin / Infineon Technologies AG

"Plasma process charging induced damage (PID) of MOS devices"

This tutorial will present a short introduction to the field of PID followed by a detailed overview of PID reliability characterization methods including stress, test structure concepts and data analysis techniques.

Over 25 years of research in the field of PID would lead to the assumption that required test structures and stress methods are well defined. However, this is not the case and the analysis of PID stress data can discover large obstacles. Further, different circuit application areas for MOS devices require different stress methods. For complex state of the art process nodes with various FET dielectric thicknesses and device types and many metal layers the number of qualification test structures can easily go up to 1000. An applied characterization method requires fast reliability stresses for the detection of PID. This is described in the tutorial as well as a suitable additional stress for a quantification of the PID event. Recent publications show the effectiveness of this method. Additionally, the tutorial focuses on the test structure design, which can have a significant effect on the PID stress results. Inappropriate layout can either introduce severe damage which is not relevant for a product or suppress relevant plasma damage leaving a dangerous blind spot in product design. Various product relevant test structures and stresses are reviewed for a complete characterization of PID during process qualification. The lack of a comprehensive PID standard in the reliability community leaves many used qualification methods with obvious gaps. Pit falls of the characterization methods and test structures as well as the relevant PID literature will be presented. Simple PID protection schemes will also be discussed which are relevant for test structure and product design.

The tutorial is aimed towards reliability engineers with some basic reliability experience in the field. Experts will enjoy the detailed case stories with "strange" PID data. A lot of hands-on material is presented which can be implemented at your work place.

Andreas Martin received his M.Eng.Sc. in Electrical and Electronic Engineering from the Technical University of Darmstadt, Germany, in 1992. After six years in the silicon technology characterisation group of the research center "Tyndall Institute" (former NMRC), Cork, Ireland he started working for the central Reliability Methodology department of Infineon Technologies AG in Munich, Germany in the field of fWLR Monitoring. He is involved in advanced and novel test structure design, development of new stress methods and data analysis techniques on the topics: dielectrics, plasma induced damage, metallisation and device degradation topics for a wide range of processing nodes. He is responsible for the PID process qualification and plasma charging design manual rules at Infineon. He has published and co-authored numerous papers/presentations, given tutorials and invited talks at various conferences and served in committees of the IEEE IRW, IEEE IRPS, ESREF and of the "Workshop on Dielectrics in Microelectronics" (WoDiM) for many years. He has published some patents and was involved in paper reviews for several journals. He is a senior member of the IEEE, Infineon's alternate of the JEDEC-subcommittee 14.2, member of the IEC WLR-workgroup TC 47 and co-chair of the German ITG-group 8.5.6 on "WLR and reliability simulations".