Steve Ramey / Intel

"Transistor reliability in the FinFET era"

With the evolution to FinFET-style transistors, there are new features that modulate traditional reliability mechanisms. For example, the vertical sidewalls are typically <110> crystal orientation, which can influence oxide quality and trap behavior. Also, in Tri-gate devices, there are corner effects that can come into play. This tutorial endeavors to provide a review of all transistor reliability mechanisms and highlight interactions associated with three-dimensional transistors. The tutorial begins with a description of transistor reliability physics and electrical behavior. It then reviews the standard reliability mechanisms such as TDDB, BTI and hot carrier, especially in relation to the Tri-gate device. Additional effects are also detailed, such as local self-heating, SILC, and variation. Throughout, examples will be shown from various Tri-gate process technologies, highlighting the impact of continued technology scaling.

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