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"A NBTI Reliability Framework from Atoms to Processors"

Negative Bias Temperature Instability (NBTI) continues to remain as a serious reliability concern in HKMG FinFETs and impacts the long term performance of CMOS circuits. It is therefore important to develop a modeling framework to estimate the NBTI limited end of life degradation in devices and the corresponding degradation in circuits for various mission profiles. Such a framework can be added to the existing Design Technology Co-Optimization (DTCO) flows for concurrent optimization of performance, power, area and aging (PPAA) of advanced CMOS chips.

In this presentation a NBTI reliability framework will be described that can estimate the impact of gate stack processes (atoms) and MOSFET architectures on circuit reliability. A BTI analysis tool will be presented that can analyse experimental data across various technologies and processes. TCAD implementation of the framework will be shown to study FinFET scaling and impact of Gate All Around (GAA) NSFET architectures having different channel materials, and check quantum confinement and strain effects on NBTI. A compact model that can handle circuit degradation under arbitrary gate activity will be discussed, with some examples of circuit degradation under actual workload versus worst case DC cases. A simulation flow will be presented to link device and RO degradation to that of processors, which includes detailed characterization of standard cells under NBTI. Several benchmark circuits will be analyzed. Finally, the statistical aspect of device-level variability and variable reliability will be addressed, and connections will be made to estimate the variability associated with SRAM performance degradation.

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