Kang-Wook Lee / SK Hynix

"Advanced Packaging Reliability"

With diminishing returns from traditional transistor scaling further improvements in power and performance of systems are likely to come from advanced packaging technologies. Furthermore, the increased focus on mobile computing, HPC, cloud networking, and AI has highlighted the need for improved form-factor, improved performance, and low power technologies. This can be achieved only via increased emphasis on advanced packaging concepts such as 2.5D/3D integration and fan-out wafer level packaging technologies. Further trend of 3D integration towards thinner chip, more layer stacking, and more joining density to maximize area efficiency. 2.5D and fan‐out packaging requires more fine width/space, multi‐layers of Cu RDL and large package size for multi‐dies integration. These trends could induce severe reliability challenges.

This session will focus on advanced packaging reliability challenges of 2.5D, 3D and fan-out packaging for topic for further system scale.

Kang-Wook Lee is currently VP, Package Development, SK Hynix, Korea. He received the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Japan, in 2000. From 2000 to 2001, he was a Researcher with Japan Science and Technology Corporation, Japan. From 2001 to 2002, he was a Postdoctoral Researcher with the Department of Electrical, Computer, and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY, USA. From 2002 to 2008, he worked with Memory Division, Samsung Electronics Ltd., Korea, as a Principal Engineer. From 2008 to 2016, he worked with the New Industry Creation Hatchery Center (NICHe), Tohoku University, Japan as a Professor. From 2017 to 2018, he worked with R&D, Amkor Technology Korea, as a VP.

He has led the development of 2.5D/3D integration technologies for high performance/density memories, multi‐functional convergence systems, fan-out wafer-level packaging for system scale, and the reliability studies about the impacts of 3D integration process on device performance. He is a Senior Member of IEEE.