Rahim Kasim / Intel Corporation

"Low-K dielectric Reliability Challenges with Technology Scaling"

Technology scaling introduces new challenges for interconnect reliability assurgent from the need for improved RC as dimensions shrink. Innovative process integration schemes that fully utilize the benefit of low-K dielectric without decreasing reliability margin are crucial to the successful certification of a leading edge processes. The combination of low-K dielectrics and dimensional scaling significantly increases the interconnect reliability risk for both intra-layer and inter-layer dielectrics. Additional process optimizations using novel patterning schemes extends Reliability challenges beyond intrinsic regime and introduces process variability as a consideration for dielectric breakdown characterization and product qualification. This Tutorial will primarily focus on TDDB (Time dependent dielectric breakdown) characterization of low-K dielectrics, breakdown physics, acceleration models and key Reliability challenges at MOL and BEOL.

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