

Moderators: Chetan Prasad (Intel Corp), Jacopo Franco (IMEC)
Workshop Attendance: 45 ± 4 attendees
Survey Responders: 22 attendees or ~ 50%

Background

In recent technology nodes with ultra-scaled 3D transistors, Hot Carrier (HC) induced degradation is fast becoming a concerning FEOL degradation mechanisms. Due to its inherent physical complexity, HC degradation requires careful experimental characterization to analyze and separate out individual components, and thorough modeling to achieve relevant reliability projections. In this workshop, we will discuss recent trends in HC literature, focusing on a list of topics related to current characterization practice, modeling approaches, and device engineering for HC mitigation, with the goal of assessing the existence of a consensus view of the reliability community on each of these aspects.

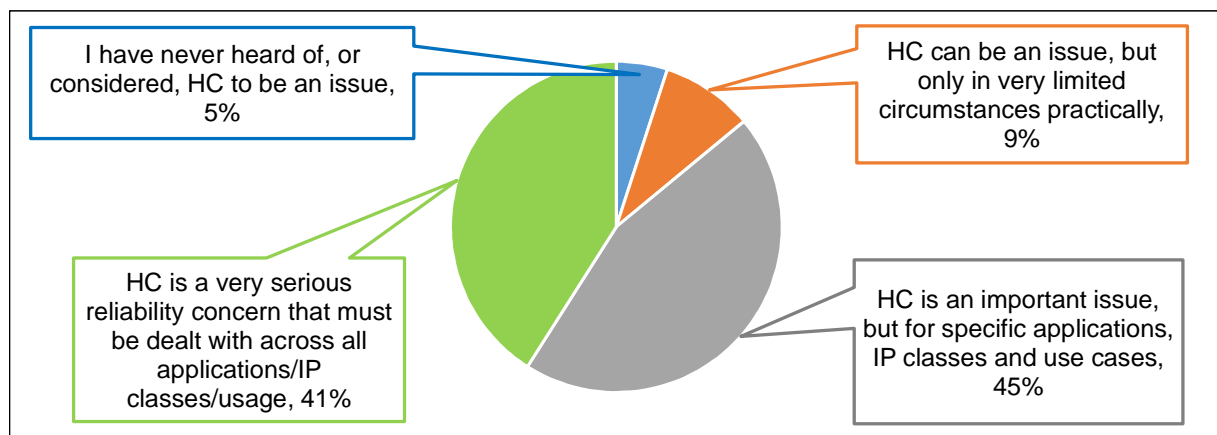
Workshop Objectives

- Survey the community, and assess HC methods, processes and concepts in current use
- Enable a discussion in the areas of testing, modeling and device engineering for HC
- Achieve (as far as possible) a consensus view on certain aspects of HC, and highlight topics of concern for future investigations.

Topics of Discussion

1. The Importance of HC induced degradation in 3D devices

Question: “HC degradation is thought of by some to be an important reliability, performance concern for 3D transistors. Which statement below would you most agree with?”

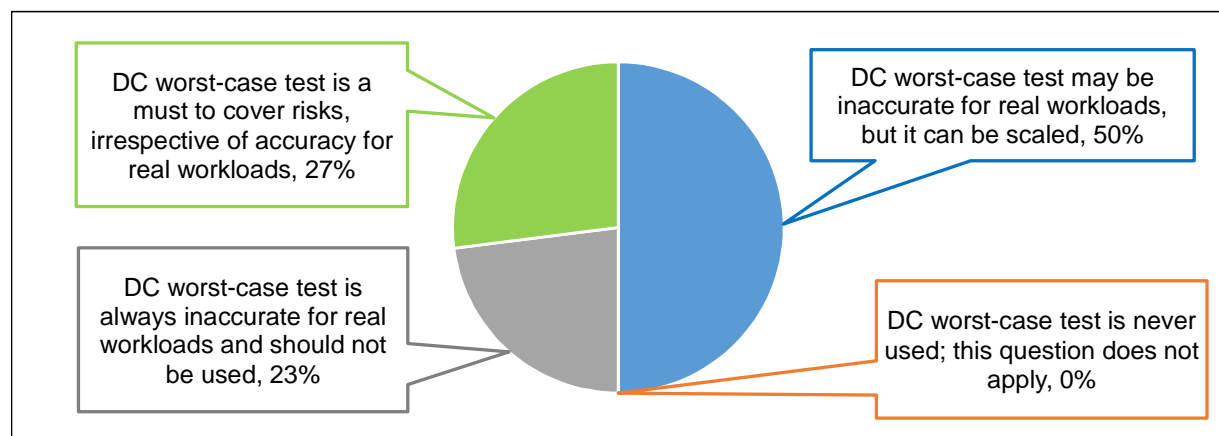


The majority of the responders agreed that HC was a serious concern that either affected some or all applications, IP classes and use scenarios. Only a small fraction believed that HC was either a non-issue, or an issue with limited impact. With this understanding, the discussion delved into the impacts of HC on various aspects of transistor reliability.

2. Standards-based Testing for HC, and its Suitability

As driven by existing qualification standards and methodologies, HC is traditionally studied at worst-case biases, i.e., maximum impact ionization, or at $V_G=V_D$: is this still enough? Does the community see a need to move toward more comprehensive studies in the whole $\{V_G, V_D\}$ bias space? Is it acceptable to simply rescale the degradation measured in DC at worst-case bias to the actual AC workload?

Question: “Standards-based testing for HC are conducted in DC mode at “worst-case” bias, such as maximum impact ionization, or $V_d=V_g$. Are these test methods appropriate?”



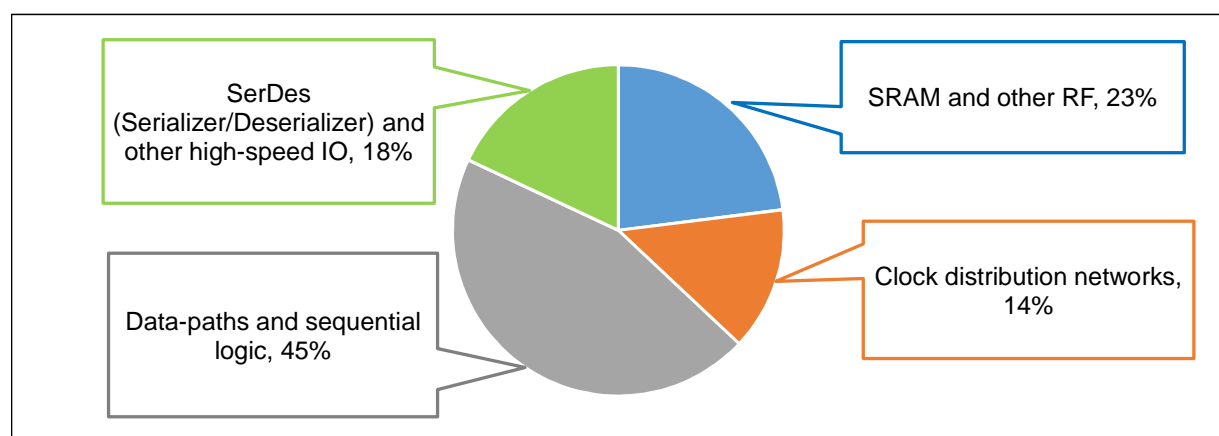
The majority of the audience believed that DC worst-case testing was a necessity that could be scaled as needed. Interestingly, a small fraction believed the test should not be used, however, were still using it.

- General Impressions
 - DC worst-case evaluations are often used as they are easy to standardize – realistic AC stress may be quite challenging to standardize.
 - However, DC stress assessments might leave some useful reliability margin behind.
 - Impact of device layout seems to not have been sufficiently explored/understood yet.
- Modeling and Physics
 - Physics-based HC models, including Single Vibrational Excitations (i.e., single highly energetic carrier) and Multi-Vibrational Excitations (i.e., many not-so-highly energetic

- carriers), that were originally developed for planar devices have already been adapted for contemporary 3D (FinFET) devices.
- Using these models, it is possible to calculate lifetime for realistic AC stress conditions based on model calibration to DC stress data.
 - From a Test Perspective
 - State-of-the-art commercial parameter analyzers allows for AC stress measurements with realistic Vg/Vd waveforms: therefore, it seems feasible to standardize AC stress conditions, comprising different stress scenarios occurring in different circuits (e.g., matrix of Vg/Vd crossing waveforms, corresponding to typical range of slew rates and fan-outs).
 - Note: circuit designers can provide accurate info on activity and slew rates for actual usage waveforms.
 - Lifetime Projections
 - For non-aggressively scaled nodes, passing traditional DC worst case qualification is still feasible; on the contrary for aggressive technology nodes, realistic AC stress cases should be necessarily considered to avoid pessimistic projections: e.g., 16nm FF Ring-Oscillator aging seems to reflect BTI kinetics, with no clear signs of HC degradation kinetics suggesting negligible HC degradation in realistic AC conditions.

With this above discussion, an additional question was posed to the audience on what classes of IP and circuitry they believed were most susceptible to HC aging and degradation.

Question: *“What classes of circuitry would you consider to be areas of concern for HC aging?”*



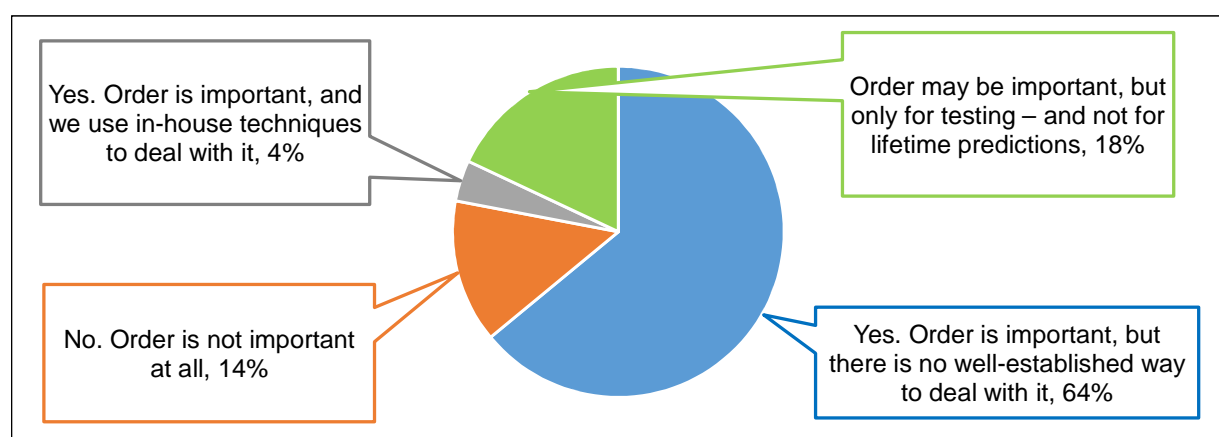
The responses for this query caused some surprise in the audience, as a significant number of respondents believed that data-paths and sequential logic were at risk – which was not what was anticipated. Additionally, the SRAM choice was contaminated by the fact that RF was ambiguous, and could mean Register File IP as well as Radio Frequency IP. Nevertheless, a surprisingly small number of respondents believed that high-speed IOs (SerDes) and clock distribution networks were at risk.

- HC degradation dependence on switching speed and frequency is not quite simple.
- From a Design Perspective
 - Clock distribution circuits, despite high frequency switching, tend to have very fast slew rates. Therefore, they may face HC stress conditions only for limited time durations, and consequently, their HC sensitivity may be lower than heavily loaded circuits at those frequencies.
 - The above potentially applies only to the lightly-loaded sections of the clock network, and maybe not the more heavily-loaded drivers.
 - On the contrary, other less fast circuits might be subject to longer HC stress due to slow slew rates, despite a lower switching activity compared to clocks.
 - The gate fan-out or load capacitance will modulate the duration of the HC window.
- IO designers in the audience affirmed that SerDes is definitely an issue, due to its very high speed of operation and loading.
- Analog designers in the audience also raised the concerns of specific circuit topologies that can experience continuous biasing in the high VD, moderate-to-high VG domain → examples are diode-like wired transistor in current mirrors, etc.
 - In such cases, worst-case DC stressing might still be relevant.

3. BTI and HC Interaction Effects – Is Order or History Important?

One area that seems relatively lightly reported on in the literature is that of interaction effects between BTI and HC. Particularly, does the bias history affect the device degradation – or, in other words; does BTI have the same impact on a device which has already suffered HC degradation vs. one which has not?

Question: “*Is the order of degradation important for 3D Transistors (such as BTI on a device with pre-existing HCD, or vice versa)?*”



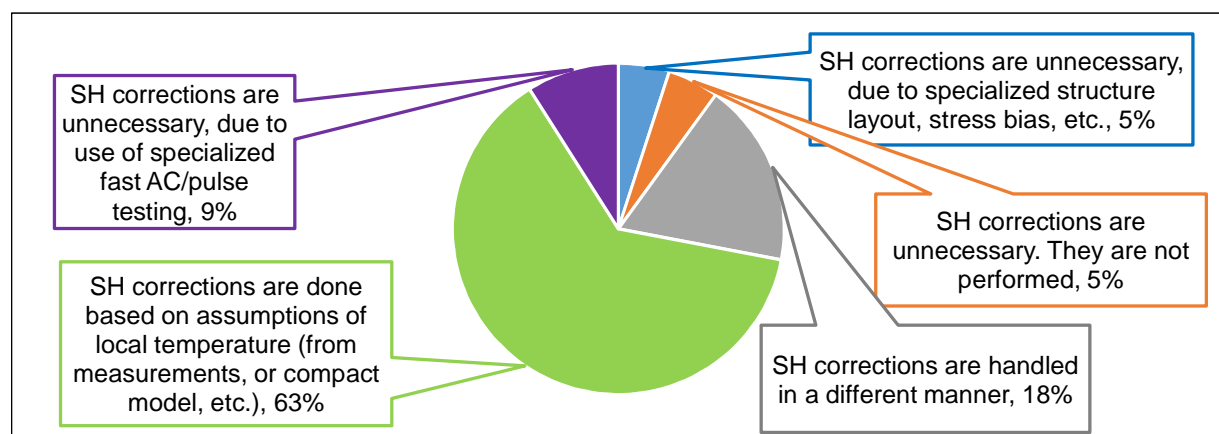
A majority of the respondents believe that order does matter, but also believe that there is really no well-established or industry-standard way to deal with this effect. A small fraction of the responders do have special in-house techniques to deal with this effect.

- Overall Consensus
 - From the perspective of quasi-static assumptions and lifetime projection, it is very important to determine whether the degradation contributed by the two mechanisms can be simply “added”, as actual workloads can be very disparate, and it would be impossible to define a single representative historic stress vector.
 - Further study seems to be necessary to determine unequivocally if history effects are present: as there have been only few contradictory reports in the literature so far.
 - Even though it might be possible to observe history effects at the single device level, at the circuit level, there are strong chances that these effects would average out, especially for high transistor count topologies. If this is true, then the problem may be more academic than practical.
 - Circuit level testing of history effects can be performed by employing ring-oscillators with enable signals in order to commute from BTI-only stress condition to HCI/BTI in various sequences.

4. Accounting for Self-Heating During HC Testing

The presence of self-heating (SH) is evident in advanced nodes with 3D devices, as has been reported extensively in the literature. Given HC testing induces significant levels of SH due to carrier flow in the channel, how can one de-embed the SH impact on HC degradation consistently across the whole {VG,VD} bias space?

Question: “Does your team account for self-heating as part of your HCD measurements? If so, how?”



A vast majority of the respondents (> 80%) use SH corrections for their HC degradation data. Most of them use corrections based on thermal modeling (either rigorous, or compact) derived from measurements of local temperatures. A smaller fraction uses other methods.

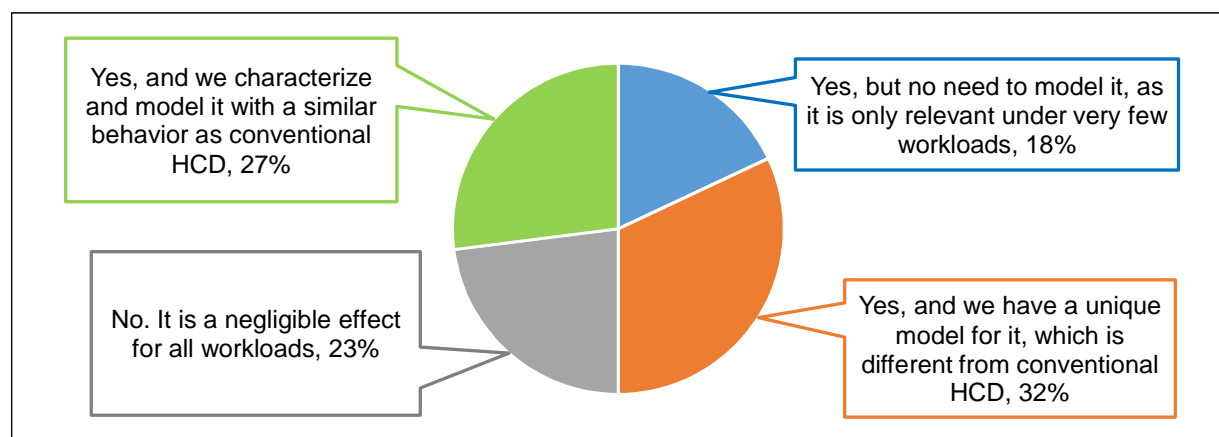
Only a very small population believe that SH is not a concern for their use scenarios and have no corrections. For planar bulk devices, this is still a valid assumption and SH is a minor concern at most if not all bias scenarios.

The rest use techniques that preclude the necessity for SH corrections – either through test structure or bias optimization, or through fast AC testing (such that SH is minor).

5. Off-state HC Degradation – Is it a concern?

Off-state HC degradation has been reported by multiple teams in the literature, and occurs in conditions where the channel is not turned on. Is this relevant for Si FinFETs? If yes, which unified failure criterion can we use for any stress {VG,VD} combination?

Question: “Are you worried or concerned about off-state HCD in 3D FinFET transistors?”



Responses for this question were evenly spread across all 4 answer choices, with no clear majority for any specific process. Roughly half the respondents consider this mode to either be an irrelevant effect for all workloads, or relevant but not worth modeling except for very specific workloads.

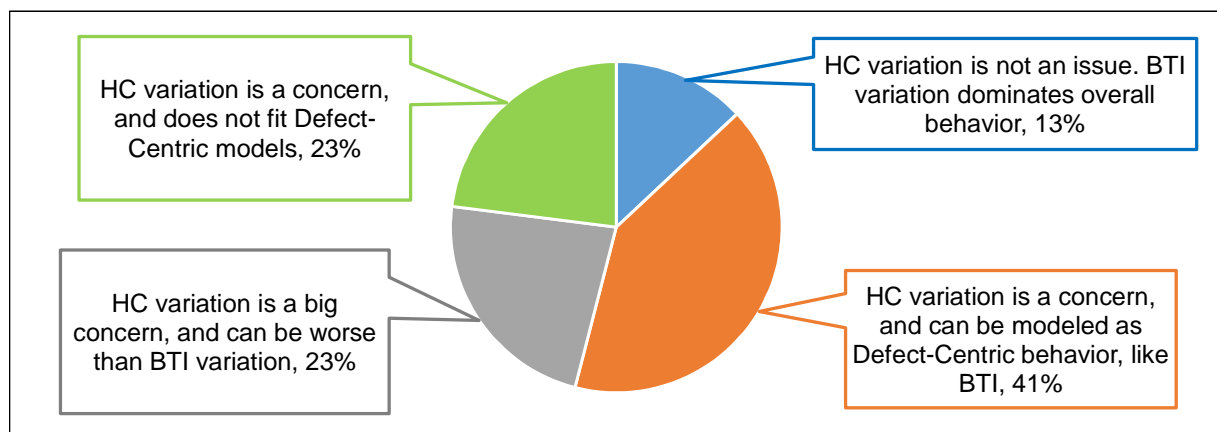
- Relevance and Physics
 - Off-state degradation is most probably not relevant for standard digital designs, but could be relevant for some analog circuitry.
 - Accelerated Vd stress conditions, combined with trap generation models, might be needed to be able to rescale off-state degradation to operating Vd.

- However, accelerated V_d conditions should be in the vicinity of nominal V_{DD} to avoid activating other extrinsic mechanisms.
- Some groups in the literature have reported off-state stresses causing the generation of oxide traps, which can then trigger oxide breakdown.
- Note: the typical shifts that are monitored (I_{dsat} and V_{th}) are usually not sufficient for off-state degradation, and other device metrics as I_{off} , SS , $GIDL$, may also need to be monitored.
- Foundry Process Qualification Aspects
 - Off-state degradation is part of the standard foundry process qualification ever since the 90nm technology node (at least).
 - This qualification looks mainly for I_{dsat} and V_{th} degradation, and if these degradations are below a certain critical level, then the technology is considered as qualified, and no dedicated off-state degradation modeling is performed.
 - Note: in many cases, I_{off} is monitored, even though it may not be listed as a qual requirement.
 - If off-state stress degradation of reasonable magnitudes is actually observed, usually the first reaction of the foundry reliability engineer is to optimize device junctions; since junction optimization for off-state reliability seems to be an easier task as compared to that for on-state hot carrier reliability.
 - After any such junction engineering, if the off-state degradation is still non-negligible, then a worst case DC degradation model is developed by stressing at high V_d with a range of low V_g conditions.

6. How important is HC variation? How could it be tested and modeled?

Is variation of the HC degradation a relevant effect? If yes, then what experimental approaches are effective to characterize it across the $\{V_G, V_D\}$ stress space, and how would we model it?

Question: “Is variation as much a concern for HCD as it is for BTI? If so, how to deal with it effectively?”



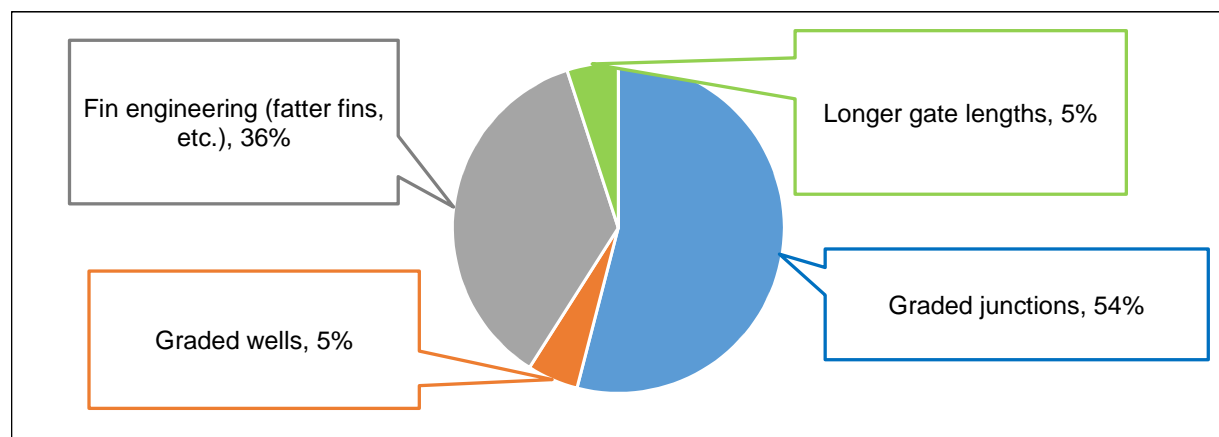
Research on BTI variation has been in the forefront recently, with advances in areas such as the Defect-Centric distribution over the last decade. The majority of respondents (87%) agree that HC variation was also a concern, but there were split opinions on whether it was comparable to, or bigger than, BTI variation, as well as on whether the Defect-Centric model could be used to model this behavior, or not.

- Importance and Relevance
 - Aging variability appears to be much more of a concern in device level studies, but seems to not be as impactful at the circuit level. This is potentially due to the averaging effect in even small circuits.
 - On these lines, HC variation is probably not very relevant, since HC is an issue for high switching rate circuits, which typically comprise many stages. Therefore, aging variations would be expected to average out.
 - Variability is very relevant for cells operating and being simulated at high-sigma points, such as SRAM cells. However, such cells, tend to have low switching activity.
- Physics and Modeling
 - Defect-Centric (or Exponential-Poisson) distribution can be used for HC-induced ΔV_{th} variability. However, HC degradation also consists of mobility reduction and series resistance increase effects, which are not captured in the DC statistical model. One would expect these terms to increase the overall HC degradation variability.
 - HC degradation is strongly localized: this aspect can have an impact on the degradation variance. Moreover, exponential distribution of single defect impacts might not be maintained up to high percentiles. Further study would be needed to clarify this aspect.
 - Time-zero variations might dominate variability: some groups have reported constant device-to-device variance, irrespective of aging (only mean value shifts). However, if the variance of the degradation is large as compared to the time zero variation, an increased variance can be observed after HC/BTI stress. For realistic mean degradation levels, time-zero variation are probably still the major concern.
- Design Aspects
 - For specific IP designers, variability is a critical concern. However it is often difficult for them to gauge whether aging variation is additive on top of time-zero variability.
 - In most cases, variance after stress is found to be similar or slightly higher than the time-zero or process variance. However, some reports describe methods to reduce variance through the correlation between time-zero performance and aging (e.g., strongest devices aging more quickly, thereby tightening the I_{dsat} distribution).

7. Device engineering strategies for HC mitigation at the transistor level

Which device design strategies are effective in tackling the challenges of HC degradation without applying undue penalties on the device performance?

Question: “What, in your opinion, are effective device design strategies to manage HCD in 3D Transistors without taking too much performance penalties?”



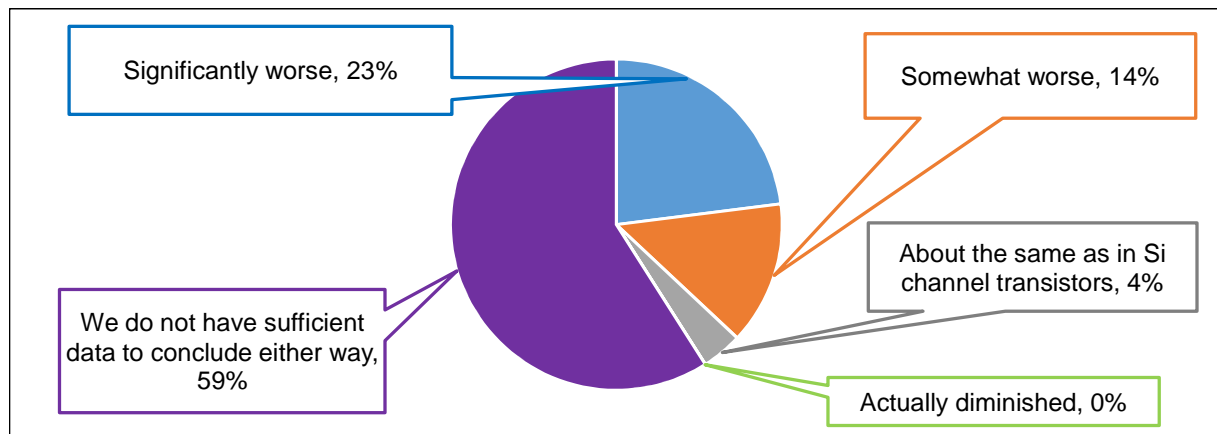
A large majority of the respondents (90%) focused on junction and fin engineering as the preferred device modulation techniques for HC mitigation. Very few believe that well engineering or longer gate lengths are viable options.

- Junction engineering always necessary for the management of HC reliability.
- Care must be taken, as HC mitigation methods can sometimes adversely affect Short-Channel Effects and Electrostatic control of the gate.
- Foundry viewpoint = It is unacceptable to trade performance for HC reliability. If junction engineering affects performance, any such losses should be made up by optimization of other aspects, in order to ensure performance targets are met as planned.

8. Impact of HC on the Transition to Novel Devices and Materials?

As scaling continues and the industry considers moving to more confined geometries and/or different material systems, what are some of the impacts on HC degradation that must be considered?

Question: “Many groups are exploring new channel materials (e.g. Ge) and geometries (e.g. GAA) for future technology nodes. What do you believe reflects HCD in these options? Will it be...”



From the responses, it was clear that no one expected HC degradation to definitely diminish in impact as we scaled to more confined or non-Si channel devices. However, the majority consensus was that we did not have enough information to conclude one way or the other – which implied that a reduction was potentially possible.

- In nanowires, SH effects are expected to become significantly worse, due to additional phonon confinement. This may drive associated degradation increases.
- One possible mitigating factor is that operating voltages are expected to push lower, so there was open discussion in the group as to whether HC would still need to be worried about?
- The consensus was: most probably yes, since some carriers can gain sufficiently high energy through electron-electron scattering effects. Also, multi-vibrational excitation modes would remain active, irrespective of VDD reductions.
- The general challenge with the assessment of HC reliability on non-Si channel novel devices was highlighted and attributed to the main limitation – a gate oxide of sufficient quality would need to be developed first.

About the Moderators



Jacopo Franco is a Principal Member of Technical Staff at imec, Belgium. He received the B.Sc. (2005) and M.Sc. (2008) in Electronic Engineering cum laude from the University of Calabria - Italy, and the Ph.D. degree in Engineering summa cum laude from KU Leuven - Belgium (2013). His research focuses on the reliability of high-mobility channel MOSFETs, on modeling of oxide traps in novel MOS gate stacks, and on time-dependent variability in nanoscale devices. He has (co-)authored 190+ publications in international journals and conference proceedings, including 20+ invited papers, 1 book, 3 book chapters, 2 international patent families. He received the Best Student Paper Award at IEEE SISC (2009), and the EDS Ph.D. Student Fellowship (2012). He is one of the recipients of the EDS Paul Rappaport Award (2011), and the Best (2012), Outstanding (2014), and Best Student (2016) Paper Awards at IRPS. He is serving as a Technical Program Committee member at IRPS, IIRW, ESREF, WoDiM conferences, and as an Editor of IEEE Transactions on Device and Materials Reliability.



Chetan Prasad is the Quality and Reliability R&D manager for the 7nm process generation at Intel Corporation. He received his B.E. (1997) in Electronics and Telecommunications Engineering from the University of Mumbai, India, and his M.S. (1999) and Ph.D. (2003) in Electrical Engineering from Arizona State University, USA. His work is focused on technology reliability research across Intel's 90nm to 14nm process generations. During his tenure at Intel, he has been the recipient of 3 Intel Achievement Awards (IAA) and 10+ Divisional Awards. He has authored/co-authored 60+ papers in international journal and conferences, including the delivery of several invited talks and tutorials, and has both awarded, as well as pending, patents. He has served on multiple Technical Program Committees at IRPS, IEDM and ESREF, has peer reviewed publications for IEEE Transactions on Electron Devices, and has contributed to multiple JEDEC standard definitions.