Session 2A - Transistors: Models and Characterization

Session Chairs: *Steve Ramey, Intel, Tibor Grasser, TUWien*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2A.1 **The Physics of NBTI: What Do We Really Know? (Invited)**
Jim Stathis, IBM

11:05 AM
2A.2 **Characterization and Physical Modeling of the Temporal Evolution of Near-Interfacial States Resulting from NBTI/PBTI in nMOS/pMOS**
T. Grasser, B. Stampfer, M. Waltl, G. Rzepa, K. Rupp, F. Schanovsky, G. Pobegen**, K. Puschkarsky***, H. Reisinger, B. O'Sullivan#, and B. Kaczer#, TU Wien, *Global TCAD Solutions, **KAI, ***Infineon, #imec*

We use detailed CV/GV measurements to study NBTI/PBTI in nMOS/pMOS transistors. We extract a unique defect band inside the SiO2 insulator, which can describe the build-up of interfacial states over time in all four combinations using our recently suggested hydrogen release model.

11:30 AM
2A.3 **Self-heating-aware CMOS Reliability Characterization Using Degradation Maps**
E. Bury, A. Chasin, B. Kaczer, K. Chuang, J. Franco, M. Simicic, P. Weckx, D. Linten, imec

Based on a large statistical dataset, obtained by measurements on dedicated FET arrays, we i) propose a methodology to identify and de-convolute the active degradation mechanisms in the device in each point of the device operating bias space, ii) apply this methodology to calculate the operating lifetime in the entire bias space and iii) build a self-heating-aware and thus geometry-independent time-to-failure map.

11:55 AM
2A.4 **Cap Layer and Multi-Work-Function Tuning Impact on TDDB / BTI in SOI FinFET Devices**
W. Liu, A. Kerber, F. Guarin and C. Ortolland, GLOBALFOUNDRIES

In this work, we report comprehensive characterization and modeling of time-dependent dielectric breakdown (TDDB) and bias temperature instability (BTI) with multi-work function tuning and a cap layer above high-k in a leading edge SOI FINFET technology.

Session 2B - SiC Reliability and Devices

Session Chairs: *Aivars Lelis, US Army Research Labs, Matteo Meneghini, University of Padova*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2B.1 **The Effects of Radiation on the Terrestrial Operation of SiC MOSFETs**
B. Akturk, CoolCad

11:05 AM
2B.2 **Reliability Studies of SiC Vertical Power MOSFETs (Invited)**
D. J. Lichtenwalner, Wolfspeed

11:30 AM
2B.3 **SiC Power MOSFET Gate Oxide Breakdown Reliability - Current Status (Invited)**
C. Cheung, NIST

11:55 AM
2B.4 **Defects Affecting SiC Power Device Reliability (Invited)**
R. Stahlbush, NRL

Session 2C - ESD/Latchup

Session Chairs: *Michael Khazhinsky, SI Labs, Gianluca Boselli, Texas Instruments*
Tuesday, March 13

10:35 AM - Session Introduction

10:40 AM
2C.1 **System level ESD and its Implications on I/O Protection (Invited)**
David Pommerenke, Missouri University of Science and Technology

11:05 AM
2C.2 **Stochastic Modeling of Air Electrostatic Discharge Parameters**
Y. Xiu, S. Sagan, A. Battini, X. Ma and E. Rosenbaum, University of Illinois, *Now with IBM*

Stochastic modeling is applied to predict the probability distribution of waveform features during air discharges. The variation in these features, even with an unvarying test condition, contributes to the probabilistic nature of soft failures. An automated air discharge tester enables the collection of sufficient data for statistical modeling.

11:30 AM
2C.3 **An Integral Injector-Victim Current Transfer Model for Latchup Design Rule Optimization**
G.Quax, T. Smedes, NXP Semiconductors

In this work, we present two models which can be used to optimize latchup design rules. The first model describes the injector-victim current transfer during negative current stresses. It includes all relevant geometrical parameters of the injector, victim, and guardring. The second model describes the trigger current of a parasitic pnp bipolar during external latchup. Both models are combined to determine accurate measures for the required well-tap distance in n-wells near injectors.

11:55 AM
2C.4 **Latchup Challenges in FinFET Technologies (Invited)**
Krzysztof Domanski, Intel

Session 3A - FEOL / MOL / BEOL Breakdown

Session Chairs: *Nagarajan Raghavan, Singapore University of Technology and Design, Andrew Kim, IBM*
Tuesday, March 13

10:35 AM - Session Introduction

1:40 PM
3A.1 **Insights into Metal Drift Induced Failure in MOL and BEOL**
C. Wu, O. Varela Pedreira, A. Leśniewska, Y. Li, I. Ciofi, Zs. Tőkei, and K. Croes, imec

Co and Cu drift induced degradation were investigated in SiO2. The failure mechanism of building-up metal in dielectrics is attributed to local metal filament nucleation and growth. Metal filament growth limits the failure times at high fields, while metal filament nucleation is more dominant at low fields. The competition between these two mechanisms and intrinsic dielectric degradation makes the collection of TTF in a wide field and temperature test window inevitable for reliable lifetime predictions.

2:05 PM
3A.2 **Time-Dependent Dielectric Breakdown Statistics in SiO_2 and HfO_2 Dielectrics: Insights from a Multi-scale Modeling Approach**
A. Padovani and L. Larcher, Università di Modena e Reggio Emilia

We use physics-based breakdown simulations to investigate the time dependent dielectric breakdown (TDDB) distributions of SiO2 and HfO2 stacks. We show that the low and thickness independent TDDB Weibull slope measured in HfO2 is originated by their intrinsic defect density and the spatially correlated defect generation process. We also demonstrate that the double slope observed in TDDB distributions of IL-HfO2 dielectric stacks is related to the stochastic nature of the bond-breakage process.

2:30 PM
3A.3 **Elapsed-Time Statistics of Successive Breakdown in the Presence of Variability for Dielectric Breakdown and RRAM applications**
E.Y. Wu, A. Kim, B. Li, and J. H. Stathis, IBM Co.

Due to the competition of multiple spots (filaments) culminating in final hard breakdown in very long wires, it is imperative to develop a comprehensive methodology to correctly incorporate this post-BD margin in technology qualification. In filamentary RRAM operation, elapsed-time statistics affects multi-level switching with multiple filaments and the endurance-related lifetime. In this work, we develop a comprehensive methodology for elapsed time statistics of successive breakdown for dielectric breakdown and RRAM applications.

2:55 PM
3A.4 **Study on Mechanism of Thermal Curing in Ultra-thin Gate Dielectrics**
Y. Mitani, Y. Higashi and Y. Nakasaki, Toshiba Corporation

In order to realize the sustainable devices, thermal curing by self-heating are attracting attention recently. In order to understand the progression of the recovery by heating, in this paper, the thermal curing of the deteriorations at both SiO2 interfaces was investigated in PFETs and NFETs. As results, the damage in PFETs can be recovered even by low temperature curing, but in the case of NFETs, the damage at SiO2/Si interface is hard to be recovered.

3:20 PM
3A.5 **New Methodology for Modelling MOL TDDB**
P. Roussel, A. Chasin, S. Demuynck, N. Horiguchi, D. Linten and A. Mocuta, imec

We report a novel time-dependent dielectric breakdown (TDDB) lifetime model which accounts for the impact of different sources of variability. We prove that the Weibull and Log¬Normal distributions normally used for FEOL and BEOL TDDB lifetime predictions respectively are not adequate for MOL TDDB analysis. Due to the many sources of variability, only a convolution of Weibull and LogNormal distributions can reconcile the intrinsic break¬down mechanism with the extra variability.

Session 3B – FOCUS SESSION: WBG Reliability Synergies and Standardization

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Tuesday, March 13

10:35 AM - Session Introduction

1:40 PM
3B.1 **Brief History of JEDEC Qualification Standards for Silicon Technology and Their Applicability to WBG Semiconductors (Invited)**
J. McPherson, Consultant

2:05 PM
3B.2 **Physical Failure Analysis Methods for Wide Band Gap Semiconductor Devices (Invited)**
A. Graff, Fraunhofer

2:30 PM
3B.3 **Challenges to Realize Highly Reliable SiC Power Device - From the Current Status and Issues of SiC Wafer (Invited)**
J. Senzaki, AIST

2:55 PM
3B.4 **Evaluation Methodology for Current Collapse Phenomena of GaN HEMTs (Invited)**
T. Sugiyama,Toshiba Corp.

3:20 PM
3B.5 **Understanding and Modeling Transient Threshold Instabilities in SiC MOSFETs (Invited)**
H. Reisinger, Infineon

Session 3C - System Reliability

Session Chairs: *Guneet Sethi, Amazon Lab 135, Rob Kwasnick, Intel*
Tuesday, March 13

1:35 PM - Session Introduction

1:40 PM
3C.1 **Managing Electrical Reliability in Consumer Systems for Improved Energy Efficiency**
V. Huard, S. Mhira, A. Barclais, X. Lecocq, F. Raugi, M. Cantournet, and A. Bravaix* STMicroelectronics, *ISEN-REER*

The paper for first time explains how to run realistic electrical reliability qualification trials at system level. Experimental dataset is fully explained by new hierarchical modeling flow. This combined approach enables further tuning of the aging margin to adapt to system usage in the field. This work paves the way to Static Adaptive Voltage Scaling qualification at system level as well as dynamic modulation of aging margin in the field so to improve energy efficiency.

2:05 PM
3C.2 **COTS Electronics Reliability for Space Applications (Invited)**
Jonny Pellish, NASA

2:30 PM
3C.3 **Machine Learning Based Dynamic Cause Maps for Condition Monitoring and Life Estimation**
A. Kale, A. Marathe, A. Kamath, N. Dhar, S. Sellers, Google

Estimating failure modes and life of electronic sub-component in field environment is challenging because of factors such as dynamic field environment, component interactions and errors and variability in operating characteristics. This paper addresses these challenge by developing dynamic cause maps using physics based models, field data and machine learning algorithms.

2:55 PM
3C.4 **Exascale Fault Tolerance Challenge and Approaches (Invited)**
Cameron McNairy, Intel

3:20 PM
3C.5 **Airplane Systems Design for Reliability & Quality (Invited)**
Anapathur Ramesh, Boeing

4:10 PM
3C.6 **Machine-Learned Assessment and Prediction of Robust Solid-State Storage System Reliability Physics**
J. Sarkar, C. Peterson, A. Sanayei, Western Digital Corporation

Reliability physics of complex fault-tolerant memory sub-system of solid-state storage is analyzed leveraging Machine Learning, enabling successful inferential and predictive SSD system reliability assessments in a pro-active manner. While being illustrative of applying Machine Learning to complex system reliability, this paper also discusses the first published method (known to the authors) for assessing individual SSD reliability under throughput acceleration.

4:35 AM
3C.7 **Statistical Modeling and Reliability Prediction for Transient Luminance Degradation of Flexible OLEDs**
H. Kim, H. Shin, J. Park, Y. Choi, J. Park, Technology Reliability, OLED Business Samsung Electronics

We, herein, propose a modified stretched exponential decay (MSED) model in the consideration of transient luminescence decay with respect to intrinsic emissive layer dependent initial luminescence and subsequent degradation over the constant current stress tests. By using the model well fitted to experimental data measured from accelerated stress tests extrapolated to user conditions, we successfully demonstrate that a MSED extracted from statistical modeling enables the precise lifetime prediction with respect to process variation and duty factor in real operation conditions.

5:00 PM
3C.8 **Reliability of MEMS Sensors Through SelfCcalibration (Invited)**
A. Lal, Cornell University

Session 3D - Product IC Reliability

Session Chairs: *Brian Pedersen, Intel, Pierre Chor-Fung Chia, Cisco*
Tuesday, March 13

4:05 PM - Session Introduction

4:10 PM
3D.1 **Resilient Automotive Products Through Process, Temperature, and Aging Compensation Schemes**
S. Mhira, V. Huard, D. Arora, P. Flatresse[*] and A. Bravaix[**], STMicroelectronics, STMicroelectronics, [*]SOITEC, [**]ISEN-REER, IM2NP,

A 32b SoC is designed in 28nm FDSOI to operate for safety-critical applications with joint Process, Temperature and Aging compensation schemes using body-bias. This work demonstrates that up to 74% energy efficiency can be gained by combining Body-Bias Process, Temperature and Aging compensation schemes altogether. This combination of compensation schemes offers the best energy efficiency gain as compared to recent results while guaranteeing high-level of robustness (<1 ppm) and safety for automotive products.

4:35 AM
3D.2 **Fast Chip Aging Prediction by Product-like V_{min} Drift Characterization on Test Structures**
S. E. Liu, G. Y. Chen[*], M. K. Chen[*], D. Yen, W. A. Kuo, C. S. Fu, Y. S. Tsai[*], M. Z. Lin, Y. H. Fang, M. J. Lin, MediaTek Inc., [*] Taiwan Semiconductor Manufacturing Company, Ltd.

We develop a novel product-like characterization methodology to predict chip aging rapidly. To assure reliability, an aging voltage guard band is usually collected by HTOL and implemented to a chip's voltage setting. We proposed a method to mimic product-like characterization on test structures to evaluate Vmin shift. Then, the correlation was established between test structure measurements and chip-level Vmin shift analysis. Therefore, product aging guard-band can be assessed rapidly with process and use condition changes.

5:00 PM
3D.3 **Reliability Characterization of Advanced CMOS Image Sensor (CIS) with 3D Stack and In-pixel DTI**
Y. Ji, J. Kim, J. Kim, M. Lee, J. Noh, T. Jeong, J. Shin, J. Kim,Y. Heo, U. Cho, H. Sagong, J. Park, Y. Choo, G. Do, H. Kang, E. Choi, D. Sun, C. Kang, S. Shin, and S. Pae, Samsung Electronics

Due to the advancement of CMOS image sensors, camera module on the mobile platform has paved way for very high quality photos and video shooting capability. In order to improve picture quality, the CIS technology has been also scaling aggressively to provide more Mega-Pixels but it also must be less susceptible and immune to noise sources, particle, and highly reliable. In this report, we'll discuss the reliability characterization done on the 3D stack sensor.

Session 3E - ESD/Latchup

Session Chairs: *Michael Khazhinsky, SI Labs, Gianluca Boselli, Texas Instruments*
Tuesday, March 13

4:05 PM - Session Introduction

4:10 PM
3E.1 **Defect-Assisted Safe Operating Area Limits and High Current Failure in Graphene FETs**
N. K. Kranthi, A. Mishra, A. Meersha, H. B. Variar and M. Shrivastava, Indian Institute of Science

In this work, a unique measurement setup, involving integration of transmission line pulse tester with Raman spectrometer, is used to investigate the pulsed safe operating area (SOA) boundary of graphene field effect transistors (GFETs). Physical insight into various SOA boundaries is given. Unique defect-assisted degradation in channel and its correlation with the carrier transport and failure is revealed. The SOA and power to fail dependency on carrier concentration and nature of carrier transport is addressed.

4:35 PM
3E.2 **On the ESD Behavior of a-Si:H based Thin-Film Transistors: Physical Insights, Design and Technological Implications**
R. Sinha, P. Bhattacharya, S. Sambandan and M. Shrivastava, Indian Institute of Science

In this work, we present detailed physical and technological insights into the ESD behavior of a-Si:H TFTs. Pre-Breakdown degradation is investigated. Device failure and effect of various parameters on failure is investigated. Effect of Channel dimensions on failure mechanism is thoroughly explored. For the first time, ESD behavior of a-Si:H based Gated diodes and Resistors is reported. Detailed Investigation on Drain Underlap devices and their possible usage as I/O protection device is discussed.

5:00 PM
3E.3 **Contact and Junction Engineering in Bulk FinFET Technology for Improved ESD/Latch-up Performance with Design Trade-offs and Its Implications on Hot Carrier Reliability**
*M. Paul, B. Sampath Kumar, H. Gossner[*] and M. Shrivastava, Indian Institute of Science, *Intel Deutschland*

Role of contact and junction engineering to improve ESD and Latch-up robustness while addressing its's implications on hot carrier reliability is discussed. Contact and junction engineering boosts ESD and latch-up robustness, however can adversely affect the HCI reliability, which has been explored in this work

keeping all ESD/Latch-up design parameters in mind. This has allowed us to derive technology guidelines for maximizing overall reliability behavior. Based on these guidelines, a hybrid contact/junction technology is proposed.

Session 4A - FEOL / MOL / BEOL Breakdown

Session Chairs: *Nagarajan Raghavan, Singapore University of Technology and Design, Andrew Kim, IBM*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4A.1 **Mechanism of Soft and Hard Breakdown in Hexagonal Boron Nitride 2D Dielectrics**
A. Ranjan, N. Raghavan, S.J. O'Shea, S. Mei, M. Bosman*, K. Shubhakar and K.L. Pey,*
*Singapore University of Technology and Design (SUTD), A*STAR*

In this study, we investigate the physical mechanism of soft and hard breakdown using conductive atomic force microscope (CAFM) as a nanoscale spectroscopy tool on blanket h-BN films with tox = 5 nm. The soft breakdown (SBD) regime involves percolation path formation with boron vacancies while the hard breakdown (HBD) regime shows nano-pitting that involves removal of h-BN layers and formation of a metallic contact due to CAFM tip adhesion with the Cu substrate.

8:30 AM
4A.2 **The Physical Mechanism Investigation of Off-State Drain Bias TDDB and its Implication in Advance HK/MG FinFETs**
I. K. Chen, S. C. Chen, S. Mukhopadhyay, D. S. Huang, J. H. Lee, Y. S. Tsai, R. Lu, J. He, Taiwan Semiconductor Manufacturing Company, Ltd.

This work presents a systematic study to understand the off-state drain bias TDDB mechanism, especially for the short channel devices in advanced FinEFT technologies. With additional process optimization such as source/drain proximity push, the sub-threshold leakage current increases, which dominates the off-state TDDB resulting in worse lifetime during practical circuit stress conditions. Impact of body bias on sub-threshold current is also studied with detailed mechanism.

8:55 AM
4A.3 **AC TDDB Extensive Study for an Enlargement of Its Impact and Benefit on Circuit Lifetime Assessment**
M. Rafik A.P. Nguyen, X. Garros*, M. Arabi, X. Federspiel, C. Diouf, ST Microelectronics, *CEA-Leti*

Abstract – With technology scaling and hardening of operating conditions requirements, Time Dependent Dielectric Breakdown (TDDB) remains a major reliability concern. In this paper we show that considering AC rather than DC TDDB would be a promising way to generate margin on lifetime assessment and also to lower the predicted impact of the breakdown on circuit functionality.

9:20 AM
4A.4 **A Systematic Study of Gate Dielectric TDDB in FinFET Technology**
H. Kim, M. Jin, H. Sagong, J. Kim, U. Jung, M. Choi, J. Park, S. Shin and S. Pae, Samsung Electronics

TDDB may have been qualified with only considering operating Ninv and Pinv, but it is necessary to consider all modes including the accumulation mode & off-state mode as well for correctly assessing product level gate oxide dppms and remove conservatism. This along with AC stresses further enables the reliability margin, otherwise, cannot be fully explained generally large gap observed between wafer-level DC based TDDB and product level HTOL, extending technology Vmax headroom without reliability tradeoffs.

9:45 AM
4A.5 **Successive Breakdown Mode of Time-Dependent Dielectric Breakdown for Cu Interconnect and Lifetime Enhancement under Dynamic Bias Stress**
S.K. Lee, K.T. Jang, S.M. Yi and Y.C. Joo, Seoul National University

In gate dielectrics, successive breakdown (BD) was caused by randomly generated bond breakages of the dielectrics. In inter-metal dielectrics, we confirmed that successive BD occurred by the formation of metallic filaments for the first time. The filaments of the successive BD are consisted of Cu atoms mediating bond breakages. Moreover, TDDB lifetime was improved under bipolar stress compared to DC and unipolar stresses due to Cu atom to ion conversion and formation of misaligned filaments.

Session 4B - GaN-based devices reliability

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4B.1 **Degradation of Vertical GaN FETs Under Gate and Drain Stress**
M. Ruzzarin, M. Meneghini, C. De Santi, M. Sun, T. Palacios*, G. Meneghesso, and E. Zanoni, University of Padova, *Massachusetts Institute of Technology*

We report the analysis of degradation of GaN VFETs under gate and drain stress. High gate bias induces the injection of electrons from the channel towards the gate dielectric (positive Vth shift) and the de-trapping of electrons from the gate insulator to the gate metal (increase in SS). The results of drain step stress reveal that the devices are stable up to VD=280 V, with no significant change in device characteristics.

8:30 AM
4B.2 **A Novel Insight of pBTI Degradation in GaN-on-Si E-mode MOSc-HEMT**
W. Vandendaele, X. Garros, T. Lorin, E. Morvan, A. Torres, R. Escoffier, MA Jaud, M. Plissonnier, F. Gaillard, CEA-Leti

GaN-on-Si HEMT technology is now considered as a serious candidate for medium power applications (650V rated). Vth instabilities are a major concern to increase lifetime of these power transistors. Advanced E-mode MOSc-HEMT (MOS-channel-HEMT) configuration has been recently introduced and studied under harsh gate conditions. In this paper we present for the first time a comparison between AC and DC stress combined with ultra-fast pBTI measurements (< 10µs) on GaN-on-Si E-mode MOSc-HEMTs.

8:55 AM
4B.3 **Reliability Issues of GaN Commercialization (Invited)**
U. Mishra, University of California, Santa Barbara

9:20 AM
4B.4 **Comprehensive Study into Underlying Mechanisms of Anomalous Gate Leakage Degradation in GaN HEMTs**
K. Mukherjee, F. Darracq, A.Curutchet, N. Malbert and N. Labat, IMS Lab, University of Bordeaux

This work investigates fundamental mechanisms governing an atypical parasitic gate leakage characteristic observed in DC forward gate behavior of Schottky gate GAN HEMTs after aging tests. DC measurements are performed to ascertain its long term impact. Detailed TCAD simulation study, for the first time to ourknowledge, reproduces this anomaly through donor state induced surface leakage and trap assisted tunneling across the AlGaN barrier. A proposed hypothesis addresses the unpredictable evolution of this effect.

9:45 AM
4B.5 **On the Origin of the Leakage Current of p-Gate AlGaN/GaN HEMTs**
*A. Stockman, E. Canato[**], M. Meneghini[**], G. Meneghesso[**], E. Zanoni[**], P. Moens and B. Bakeroot**
*ON Semiconductor, *CMST imec / Ghent University, [**]University of Padova*

Temperature dependent DC and double pulse measurements are performed on p-GaN gated AlGaN/GaN enhancement mode power transistors. Devices with improved Schottky metal barrier and p-GaN sidewall passivation are studied. It is shown that both processes reduce the reverse and forward gate leakage current significantly. Under double pulsed testing, a positive threshold shift at high forward gate voltage is induced, which is explained by electron trapping in the barrier.

Session 4C - Soft Error

Session Chairs: *Marta Bagatin, University of Padova, Nihaar Mahatme, NXP Semiconductors*
Wednesday, March 14

8:00 AM - Session Introduction

8:05 AM
4C.1 **Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs**
B. Narasimham, S. Gupta, D. Reed, J. K. Wang, N. Hendrickson and H. Taufique, Broadcom Ltd.

SRAM SER measurements across technology nodes indicate that while scaling from planar to the first FinFET process provided a large reduction in per-bit SER, the subsequent scaling within FinFET process nodes results in SER reduction comparable to per-bit cell area reduction. Extensive SER measurements over a range of voltages show a strong exponential increase in the SER of FinFET processes with reduction in bias, compared to a linear bias dependence for the planar process.

8:30 AM

4C.2 **Soft Errors in 7nm FinFET SRAMs with Integrated Fan-out Packaging**

Y. Pin Fang and A.S. Oates, Taiwan Semiconductor Manufacturing Company

The susceptibility of alpha induced soft error rate (SER) is dominated by extrinsic alpha sources in packaging such as lead-bearing solder, and bumping materials. Using wafer-level integrated fan-out (InFO) packaging technology, alpha particles emitted from extrinsic packaging materials can be blocked by redistribution layers (RDL) in InFO packaging, leaving the SER susceptibility due to intrinsic alpha sources in Si process. With technology scaling, voltage dependent SER due to intrinsic alpha particles as well as high-energy neutrons is significantly reduced in 7nm SRAM.

8:55 AM

4C.3 **Threshold Ion Parameters of Line-Type Soft-Errors in Biased Thin-BOX SOI SRAMs: Difference between Sensitivities to Terrestrial and Space Radiation**

C. Chung, D. Kobayashi, and K. Hirose, University of Tokyo and Institute of Space and Astronautical Science

Thin-BOX SOI technology is drawing attention for its low soft error sensitivity. Terrestrial radiation tests already demonstrated its further reduction under a back-bias condition. However, recent heavy ion tests with SRAMs exhibited the opposite result, a 100-fold increase accompanying 10-bits-long line-type multi-cell upsets, when they were biased. A metal bridge model suggests that this difference in response to the back-bias conditioning stems from the difference in ion parameters such as range and linear energy transfer.

9:20 AM

4C.4 **Impact of Supply Voltage and Particle LET on the Soft Error Rate of Logic Circuits**

H. Jiang, H. Zhang, R. C. Harrington, J. A. Maharrey, J. S. Kauppila, L. W. Massengill, and B. L. Bhuva, Vanderbilt University

Heavy-ion irradiations of 14/16-nm node bulk FinFET combinational logic circuits under different supply voltage and frequency are investigated. Results indicate that particle LET strongly affects logic soft-error rate (SER). Singe-event transient (SET) experimental data and models for logic SER are used to explain the differences in SER for low-LET particles and high-LET particles.

9:45 AM

4C.5 **Evaluation of the System-Level SER Performance of Gigabit Ethernet Transceiver Devices**

B. Narasimham, T. Wu, J. K. Wang, B. Conway, Broadcom Ltd.

System-level SER measurements were conducted on two Gigabit Ethernet transceiver devices designed in 28-nm CMOS process to evaluate the true impact of soft error upsets. Measurement results are compared with the system SER estimates based on test chip data for memory and flip-flop SER. Results indicate that most SEUs cause packet errors which are recoverable while the SER for more severe link-drop type events is significantly lower than estimates.

Session 4D - FOCUS SESSION: 3D/2.5D/Packaging/MEMS

Session Chairs: *Kothandaraman Chandrasekara, IBM, Sudarshan Rangaraj, Amazon Lab 126*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4D.1 **High-Density Fan-Out Technology for Advanced SiP and Heterogeneous Integration (Invited)**
K. Lee, Amkor

11:00 AM
4D.2 **Intra- and Inter-Chip Electrical Interconnection Formation by DSA (Invited)**
M. Mariappan, Tohuku University

11:25 AM
4D.3 **Stress Mitigation of 3D-packaging Induced Stresses (Invited)**
C. Croes, imec

11:50 AM
4D.4 **Fine Pitch 3D Interconnections with Hybrid Bonding Technology: Process Robustness and Reliability Results (Invited)**
L. Arnaud, CEA /LETI

12:15 PM
4D.5 **Reliability Concerns for Advanced Packaging (Invited)**
S. Iyer, UCLA

Session 4E - GaN-based devices robustness

Session Chairs: *Sandeep Bahl, Texas Instruments, Matteo Meneghini, University of Padova*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4E.1 **p-GaN gate reliability including short-circuit robustness (Invited)**
A. Castelazzi, University of Nottigham

11:00 AM
4E.2 **Lifetime evaluation for Hybrid-Drain-embedded Gate Injection Transistor (HD-GIT) under practical switching operations**
A. Ikoshi, M. Toki, H. Yamagiwa, D. Arisawa, M. Hikita, K. Suzuki, M. Yanagihara, Y. Uemoto, K. Tanaka and T. Ueda, Panasonic Corporation

The GaN transistors' reliability under continuous switching operation is a very important topic. We perform dynamic high-temperature operating lifetime (D-HTOL) test on Hybrid-Drain-embedded Gate Injection Transistors (HD-GITs) with varying input voltage, switching current and temperature to extract their acceleration factors on the switching lifetime of HD-GITs. The obtained factors are employed to estimate

the lifetime when they are used for a totem-pole power factor correction circuit to conclude that the estimated lifetime is sufficiently long.

11:25 AM
4E.3 **Safe Operating Area (SOA) Reliability of Polarization Super Junction (PSJ) GaN FETs**
*B. Shankar, A. Soni, S.D. Gupta, S. Yagi[*], H. Kawai[*], V. Unni[**], A.Nakajima**, M. Shrivastava, and E. M. Sankara Narayanan[**], Indian Institute of Science, [*]Powdec K.K., **University of Sheffield*

This work reports Safe Operating Area assessment and degradation physics in Polarization Super Junction (PSJ) based GaN FETs made in Silicon and Sapphire substrates under high voltage and high current injection conditions. Impact of device design parameters on SOA, associated trap assisted device degradation and thermal failure are studied. Correlation between polarization super junction length and failure threshold is discovered, beside power and field dependence of SOA boundary.

11:50 AM
4E.4 **On the Trap Assisted Stress Induced Safe Operating Area Limits of AlGaN/GaN HEMTs**
B. Shankar, A. Soni, S. Dutta Gupta, R. Sengupta, H. Khand, N. Mohan, S. Raghavan and M. Shrivastava, Indian Institute of Science

This experimental study reports a systematic investigation of Safe Operating Area limits in AlGaN/GaN HEMT using sub-us pulse characterization with on-the-fly Raman and CV characterization to probe defect and stress evolution across the device. Influence of a recess depth on SOA boundary is analyzed. Post failure analysis corroborates well with the failure physics unveiled in this work.

12:15 PM
4E.5 **Reliable and Damage-Resistant Optics and Detectors for X-Ray Free-electron Lasers (Invited)**
S. Hau-Riege, Lawrence Livermore National Labs

X-ray free-electron lasers (XFELs) are revolutionizing the physical and life sciences. The sweeping recent success of XFELs can be attributed to their extreme output characteristics: XFELs deliver x-ray photon pulses that are more than nine orders of magnitude brighter than any previous laboratory light source, like synchrotrons. Such extreme radiation poses a particular challenge for the short- and long-term reliability of x-ray optics and detectors which are required to steer, condition, and diagnose individual x-ray pulses. In this presentation, we will discuss how we overcame the challenges of designing damage-resistant optics and detectors without ever having had access to such radiation.

Session 4F - Metallization Reliability

Session Chairs: *Gavin Hall, ON Semi, Zsolt Tokei, IMEC*
Wednesday, March 14

10:30 AM - Session Introduction

10:35 AM
4F.1 **Next Generation Interconnect Reliability Metallization Integration (Invited)**
C-K Hu, IBM

11:00 AM
4F.2 **Electromigration-Induced Backflow Stresses in Cu(Mn) Interconnects Analyzed Based on High Statistical Sampling**
M. Kraatz, C. Sander, A. Clausner, M. Hauschildt, M. Gall, and E. Zschech*
*Fraunhofer Institute for Ceramic Technologies and Systems IKTS, *GLOBALFOUNDRIES LLC & Co. KG,*

Using an alternate Wheatstone bridge setup, sampling over a total of 800 Cu(Mn) interconnects resulted in very smooth resistance vs. time curves during the electromigration process. The test temperature was 350 °C and several current densities ranging from 13 to 17 mA/μm² were applied. Using the averaged resistance curves, linear drift portions were extracted and saturation resistances were extrapolated. The data was further analyzed to obtain a critical Blech product of (510 ± 110) mA/μm.

11:25 AM
4F.3 **Electromigration Characteristics of Power Grid Like Strcutures**
B. Li, A. Ki, P. McLaughlin, B. Linder and C. Christiansen, IBM Systems

Setting appropriate EM limit becomes more and more critical for the leading edge technologies, especially for on-chip power grid. This paper presents EM characteristics of power grid like structures. It demonstrates that the EM reliability is much enhanced from the power grid design environment comparing to the traditional single link EM structures. Discussions are made on the contributing factors to this EM reliability enhancement and how they should be utilized.

11:50 AM
4F.4 **Effect of Metal Line Width on Electromigration of BEOL Cu Interconnects**
S. Choi, C. Christiansen, L. Cao, J. Zhang, R. Filippi Jr., T. Shen, K. B. Yeap, S. Ogden, H. Zhang, B. Fu, P. Justison, GLOBALFOUNDRIES

Electromigration reliability of BEOL Cu interconnects with various metal line widths and via sizes has been studied. EM lifetime improves from minimum width to three times the minimum width, and then saturates. The proposed mechanism for EM lifetime improvement is larger grains in wider lines leading to a reduction in grain boundary diffusion. Cu grain size and Cu drift velocity were correlated to the EM lifetime behavior.

12:15 PM
4F.5 **Protective Nanometer Films for Reliable Cu-Cu Connections (Invited)**
T. Berthold, G. Benstetter, W. Frammelsberger, M. Bogner, R. Rodríguez, M. Nafría, Autonomous University of Barcelona, and Deggendorf Institute of Technology

Session 5A - Transistors: Models and Characterization

Session Chairs: *Steve Ramey, Intel, Tibor Grasser, TUWien*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM
5A.1 **Hot Electron and Hot Hole Induced Degradation of SiGe p-FinFETs Studied by Degradation Maps in the Entire Bias Space**
J. Franco, B. Kaczer, A. Chasin, E. Bury, D. Linten, imec

We study hot carrier degradation in $Si_{0.75}Ge_{0.25}$ p-FinFETs by measuring degradation maps in the entire bias space, and compare with Si counterparts. Hot carrier effects are enhanced in SiGe due to larger hole mean free path, and enhanced generation of secondary electrons in the reduced bandgap semiconductor. Both hole and electron injections are observed, partially compensating at some stress biases. Even at logic operating voltages, off-state stress increases the channel leakage due to hot-electron-induced punch-through.

2:45 PM
5A.2 **Role of Electron and Hole Trapping in Degradation and Breakdown of Oxide Films (Invited)**
A. Shluger, University College, London

3:10 PM
5A.3 **Impact of Slow and Fast Oxide Traps on $In_{0.53}Ga_{0.47}$ As Device Operation Studied Using CET aps**
V. Putcha[(1,2)], J. Franco[(2)], A. Vais[(2)], B. Kaczer[(2)], S. Sioncke[(2)], D. Linten[(2)] and G. Groeseneken[(1,2)]
[(1)]ESAT department, KU Leuven, [(2)]IMEC

Kinetics of charge trapping in the InGaAs/Al2O3/HfO2 gate-stack is studied using CET maps. A first defect population with relatively higher capture and emission energy barriers is found to affect the long term reliability of the device, while a second population with relatively smaller capture and emission energy barriers affects the device stability under high frequency operation. We conclude, it is essential to study both defect populations for accurately estimating device lifetime under different operating applications.

3:55 PM
5A.4 **PBTI in InGaAs MOS Capacitors with Al_2O_3/HfO_2/TiN gate stacks: Interface-state Generation**
E. Cartier, M. M. Frank, T. Ando, J. Rozen and V. Narayanan, IBM Research Division, T.J. Watson Research Center

Using devices with well passivated interfaces and reduced electron trapping it is demonstrated that significant interface-state generation occurs during PBTI stress in InGaAs MOS capacitors with Al_2O_3/HfO_2/TiN gate stacks. These observations on capacitors imply that the impact of interface-state generation on mobility and subthreshold degradation need to be monitored in III-V nFET once the electron trapping is brought under control.

4:20 PM
5A.5 **Reliability of Next-Generation Field-Effect Transistors with Transition Metal Dichalcogenides**
Y.Y. Illarionov, A.J. Molina Mendoza, M. Waltl, T. Knobloch, M.M. Furchi, T. Mueller and T. Grasser, TU Wien, *also with Ioffe Physical-Technical Institute*

We perform a detailed reliability study of MoS_2, MoSe2, $MoTe_2$ and WS_2 FETs fabricated on the same SiO2/Si substrate and compare the hysteresis and BTI dynamics for these devices. Our results show that the observed differences can be partially explained by the alignment of the band edges of the 2D semiconductors with the defect bands in SiO2. As such, our study provides strong fundamental insights into the understanding of the reliability of these new technologies.

4:45 PM
5A.6 **Hot Carrier Degradation, TDDB, and 1/f Noise in Poly-Si Tri-gate Nanowire Transistor**
Y. Yoshimura, K. Ota and M. Saitoh, Toshiba Corporation

We study various reliabilities in poly-Si nanowire transistors. Unique hot carrier degradation characteristics are found at low stress gate voltage where degradation was reduced due to suppressed drain avalanche hot carrier by grain boundary. Time dependent dielectric breakdown shows enhanced breakdown probability at nanowire corner similar to SOI nanowire transistors, while breakdown-time distributions is related to randomly oriented grain surface. 1/f noise shows conventional size dependence, while noise amplitude is related to grain size.

Session 5B - 3D/2.5D/Packaging/MEMS

Session Chairs: *Kothandaraman Chandrasekara, IBM, Sudarshan Rangaraj, Amazon Lab 126*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM
5B.1 **Analysis of 28 nm SRAM Cell Stability Under Mechanical Load Applied by Nanoindentation**

A. Clausner[1], G. Kurz, M. Otto*, J. Paul*, K.-U. Gierin**, J. Warmuth**, R. Jancke**, A. Aal#, M. Gal, and E. Zschech, Fraunhofer Institute for Ceramic Technologies and Systems IKTS, *GLOBALFOUNDRIES LLC & Co. KG, **Fraunhofer Institute for Integrated Circuits IIS, Engineering of Adaptive Systems EAS, #Volkswagen AG*

28 nm high-k metal gate CMOS SRAM circuits were subjected to controlled mechanical load by nanoindentation. This enables high stress fields in the vicinity of operational SRAM cells. It was found that the loading leads to an increase of the bit cell fail probability around the nanoindentation point. The results attained here provide a quantitative estimate about the influence of package-related stress on performance and reliability of microelectronic products, shedding light on CPI- and CBI-effects.

2:45 PM
5B.2 **Electromigration of multi-solder ball test structures**
C. Hau-Riege, H. Xu, Y.-W. Yau, M. Kakade, J. Li, X. Zhang, H. Farr, Qualcomm Technologies, Inc., *Qualitau,*

This study investigates the electromigration failure characteristics for wafer-level packaging multi-ball structures with different ball numbers, trace sizes, and current distributions. Unlike single-interconnect structures, the resistance and voltage measurements of multi-ball structures show distinct steps and inflections, corresponding to individual ball fails, which was confirmed through failure analysis. Electromigration performance is greatly enhanced by splitting current amongst balls and by increasing the trace size.

3:10 PM
5B.3 **Reliability Challenges in 2.5D Packaging and Embedded Silicon Bridge (Invited)**
E. Armagan, Intel

3:55 PM
5B.4 **Reliability Challenges on 2.5D/3D Chip Integration - an Overview (Invited)**
C. S. Premachandran, GLOBALFOUNDRIES

4:20 PM
5B.5 **TSV Process-Induced MOS Reliability Degradation**
Y. Li, M. Stucchi, S. Van Huylenbroeck, G. Van Der Plas, G. Beyer, E. Beyne, K. Croes, imec

Process-induced MOS capacitor reliability degradation is investigated for both “via-last” and “via-middle” TSV flows. It is shown that during via-last TSV processing, the MOS capacitor reliability is impacted by both the TSV liner open dry etch and the PVD metal barrier deposition. With a protection PN diode, the MOS reliability degradation can however be prevented. In comparison, the reliability degradation in a via-middle flow, caused by the backside TSV dry-etch reveal process, is negligible.

4:45 PM
5B.6 **Device Reliability for CMOS Image Sensors with Backside TSVs**
J.P. Gambino, H. Soleimani, I. Rahim, B. Riebeek, L. Sheng, H. Truong, G. Hall, R. Jerome, D. Price, ON Semiconductor

In this study, device reliability is characterized for two different 0.18 um BSI image sensor technologies. We show that for devices with an SiO2 liner over the gates and with SiN backside dielectrics, the backside processing can degrade device reliability (due to hydrogen depassivation) and that backside process optimization is required to achieve acceptable device reliability (to allow effective repassivation during the final hydrogen anneal).

Session 5C - Circuit Reliability/Aging

Session Chairs: *Chris Kim, University of Minnesota, Georgios Konstadinidis, Google*
Wednesday, March 14

2:15 PM - Session Introduction

2:20 PM
5C.1 **Recent Advances in In-situ and In-field Aging Monitoring and Compensation for Integrated Circuits Monitoring and Compensation for Integrated Circuits (Invited)**
M. Seok, Columbia University

2:45 PM
5C.2 **All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits**
*G. Park, *B. Kim, M. Kim, **V. Reddy, C. H. Kim, University of Minnesota, *Nanyang Technological University, **Texas Instruments*

Using simple on-chip monitoring circuits, we precisely characterized the impact of hot carrier injection and bias temperature instability aging on frequency and phase noise degradation of a 65nm all-digital PLL circuit. Experimental data shows that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. Results show that applying high temperature annealing can recover most of the phase noise degradation.

3:10 PM

5C.3 **Design of Aging Aware 5 Gbps LVDS Transmitter for Automotive Applications**

S. Jagannathan, K. Abhishek, T. Goyal, N. Mahatme, G. Easwaran, NXP Semiconductors

This work investigates the effect of circuit aging on 5 Gbps LVDS Transmitter (TX) used in automotive SoCs. A sensitivity analysis of sub-blocks is discussed. imulations suggest aging induced minor increase in Vth results in system failure. On-chip aging adaptive capability is achieved using jitter and duty-cycle correction circuity to recover critical TX performance within its specifications. Experiments confirms the efficacy of mitigation techniques, with TX restoring its performance to <5% from its pre-aging values.

3:55 PM

5C.4 **Reliability Perspective of Resistive Synaptic Devices on the Neuromorphic System Performance (Invited)**

S. Yu, Arizona State University

4:20 PM

5C.5 **Accelerated BTI Degradation under Stochastic TDDB Effect**

D. Patra, A. Kamal Reza,, M. Katoozi**, E. H. Cannon**, K. Roy*, Y. Cao, Arizona State University, *Purdue University, **Boeing Research & Technology*

The generation of new traps during TDDB may significantly accelerate BTI, since these traps are close to the dielectric-Si interface in scaled technology. This work confirms this correlation with 28nm measurement data. Based on stochastic trapping/detrapping mechanism, new compact BTI models are developed and verified with 14nm FinFET and 28nm data. Moreover, these models are implemented into circuit simulation, illustrating a significant increase in failure rate due to accelerated BTI.

4:45 PM

5C.6 **Investigation of Accuracy of Speed Sensors for Process and Aging Compensation**

R. Shah, F. Cacho, D. Arora, S. Mhira, V. Huard, L. Anghel, STMicroelectronics, *TIMA*

This paper presents experimental results of different speed sensors that can be used for process and aging compensa-tion. Replica of critical path in ring oscillator, and a dedicated design of a sub-set functional critical path are compared with regard to microprocessor speed for reference. Measurements are performed on large sample sets for varied range of temperatures. Accuracy of speed compared to reference circuit to be monitored is discussed.

Wednesday Evening – Posters
Wednesday, March 14
6:00 PM – 9:00 PM

3D/2.5D/Packaging/MEMS

P-3D.1 **Optimal Design of Dummy Ball Array in Wafer Level Package to Improve Board Level Thermal Cycle Reliability (BLR)**
S. Jeong, J. Kim, A. Kim, B. Kim, M. Lee, J. Chang, H. Kang, S. Shin, and S. Pae, Samsung Electronics*

This paper investigates the effect of dummy ball on the board level reliability by performing thermal cycling test for 5 wafer level package products. The single dummy ball array at the chip corner boosted the BLR TC performance by 30~40% and the double dummy ball array by 92%. To maximize the dummy ball effect, the dummy ball array in the chip corners should be symmetric and co-optimized with die and package size.

Circuit Reliability/Aging

P-CR.1 **Study of Impact of BTI's Local Layout Effect Including Recovery Effect on Various Standard-Cells in 10nm FinFET**
M. Igarashi, Y. Uchida, Y. Takazawa, Y. Tsukamoto, K. Shibutani and K. Nii, Renesas Electronics Corp.

This paper presents impact of Local Layout Effect (LLE) of BTI on logic circuit by measuring Ring-Oscillators (RO) consisted with many kinds of standard cells in 10nm FinFET process. The measured Tpd degradation of all ROs are well correlated with estimated one without considering LLE of BTI and its maximum error rates is -16% and +13%. The LLE on BTI recovery effect is also evaluated and there is no obvious standard cell type dependency.

P-CR.2 **A Multi-bits/cell PUF Using Analog Breakdown Positions in CMOS**
K. H. Chuang, E. Bury, R. Degraeve*, B. Kaczer*, T. Kallstenius*, G. Groeseneken, D. Linten*, and I. Verbauwhede, imec-COSIC/ESAT , KU Leuven,* imec*

The breakdown position in a MOSFET is uniformly distributed, which can be utilized to generate multi-bit entropy out of a single transistor. A dedicated test structure for this analog-BD PUF was designed and fabricated in a commercial 40nm CMOS technology.The experiment and statistical analysis has shown that the analog-BD PUF is capable for multi-bit entropy generation but it requires significant improvement to replace the binary BD-PUF demonstrated in our previous work.

P-CR.3 **New Insights into the HCI Degradation of Pass-gate Transistor in Advanced FinFET Technology**
P. Ren, C. Liu, S. Wan, J. Zhang, Z. Yu*, N. Liu, Y. Sun, R. Wang*, C. Zhan, Z. Gan, W. Wong, Y. Xia and R. Huang*, Hisilicon Technologies Co., LTD, * Peking University*

HCI degradation of pass-gate transistor with forward and reverse stress biases in advanced FinFET technology is investigated comprehensively. Due to the bidirectional stress, pass-gate HCI shows larger degradation than conventional HCI, which can induce up to 50% error in predicting pass-gate delay degradation. Based on the proposed underlying physics, compact model of pass-gate HCI is developed and verified. With further analysis on circuit level, new simulation methodology is demonstrated.

P-CR.4 **Device-level Variability Tolerance of a RRAM-based Self-Organizing Neuromorphic System**

M. Pedro, J. Martin-Martinez, E. Miranda, M.B. Gonzalez, R. Rodriguez, F. Campabadal*, M.Nafria, Autonomous University of Barcelona, *Institut de Microelectronica de Barcelona*

Device modelling and system-level simulations are needed to verify neuromorphic systems tolerance to variability. In the present work, RRAM devices have been characterized and modelled for the implementation of a self-organizing simulated crossbar array. An unsupervised learning algorithm has been applied to the system for a simple image processing application, in order to provide a proof-of-concept of the proposed bio-inspired system tolerance to device-level variability.

P-CR.5 **Reliability Assessment of 4GSP/S Interleaved SAR ADC Reliability**
R. Lajmi, F. Cacho, O. David, J-P. Blanc, E. Rouat, S. Haendler, P. Benech, E. Lauga Larroze*, S. Bourdel*, STMicroelectronics, *IMEP-LAHC–Univ.Grenoble Alpes*

Inter-leaved Successive-Approximation-Register (ISAR) Analog to Digital Converter (ADC) are widely used because they have good tradeoff between high performance sampling rate, effective resolution, power and small area in GHz range.After presenting the design content, experimental results of aging at 40°C and 125°C are shown. Then, the analysis of reliability for all the critical blocks of the ADC is discussed, i.e. switches in capacitor array, comparator and latch.

P-CR.6 **Weighted Time Lag Plot Defect Parameter Extraction and GPU-based BTI Modeling for BTI Variability**
V. M. van Santen, J. Diaz-Fortuny, H. Amrouch, J. Martin-Martinez*, R. Rodriguez*, R. Castro-Lopez**, E. Roca**, Francisco V. Fernandez**, J. Henkel and M. Nafria*, Karlsruhe Institute of Technology (KIT), * Universitat Autonoma de Barcelona (UAB), **IMSE-CNM, CSIC/Universidad de Sevilla*

We present a novel BTI variability defect parameter extraction, which filters noise and RTN with the weighted time lag plot method (previously only used to characterize RTN) to obtain a noise-free BTI waveform and then extracts BTI defect parameters. Additionally, our novel high-performance parallel graphic card (GPU) based implementation of defect-centric PDO model. Together they tackle the challenge of characterizing and modeling BTI variability to ultimately evaluate BTI variability in circuits.

ESD/Latchup

P-EL.1 **A Case Study of ESD Trigger Circuit: Time-out and Stability**
K.-H. Meng, M. Moosa, C. Torres and J. Miller, NXP Semiconductors

This paper demonstrates the use of ETT (ESD trigger circuit time-out) measurement technique and AC loop-gain analysis to investigate the root-cause of oscillation in ESD trigger circuit (TC) design in 16nm Fin-FET technology. Measurement and simulation results are presented to investigate stickiness (TC's inability to time-out) and instability of different ESD TC designs by combining the complimentary analysis tools of transient ETT simulation and AC loop-gain analysis.

Failure Analysis

P-FA.1 **A Research Study on Unsupervised Machine Learning Algorithms for Early Fault Detection in Predictive Maintenance**
N. Amruthnath, DENSO Manufacturing Michigan

Fault detection being one of the key components of predictive maintenance, it is very much needed for industries to detect faults early and accurately. In this paper, we have chosen a simple vibration data collected from an exhaust fan, and have tried to fit different unsupervised learning algorithms to test its accuracy, performance and robustness. In the end, we have proposed a methodology to benchmark different algorithms and choosing the final model

Dielectrics - Gate, MOL, BEOL

P-GD.1 **New Insight on TDDB Area Scaling Methodology of Non-Poisson Systems**
T. Shen, K. B. Yeap, S. Ogden, C. Christiansen and P. Justison, GLOBALFOUNDRIES

Because of the large spatial variations across the wafer, the Poisson area scaling law is generally inapplicable. In this work, we demonstrate that although the previous non-Poisson statistical models may match with experimental data well, they are too conservative when projecting to the actual product area. A revised area scaling approach is proposed for a more aggressive yet more accurate fail rate projection that is essential for modern technologies.

P-GD.10 **Method to Assess the Impact of LER and Spacing Variation on BEOL Dielectric Reliability using 2D-Field Simulations for <20nm Spacing**
D. Kocaay, P. Roussel, K. Croes, I. Ciofi, A. Lesniewska and I. De Wolf, imec and KU Leuven

We developed a new 2D-model to quantify the impact of LER and spacing variations. We see that existing 1D-models are a good approximation down to 20nm spacing, but at lower spacings, 2D-models will be needed. Down to the 10nm spacing, our 2D-model gives reliable predictions and allows to define specifications of LER and spacing variation for advanced BEOL-spacings. Below 10nm spacing, when local field enhancements become too high, new models will need to be developed.

P-GD.2 **Reliability Evaluation of Defect Accounted Time-Dependent Dielectric Breakdown with Competing-Mixture Distribution**
S. Yokogawa and K. Tate, The University of Electro-Communications

Defect impacts to the whole lifetime distribution of time-dependent dielectric breakdown (TDDB) are discussed statistically by using a combination model of the competing risk and the mixture. The competing-mixture distribution well explains observations of TDDB lifetime. The model is able to describe realistic bathtub behaviors of failure rate without physical inconsistencies. Understanding the behavior of the failure rate supports the estimation of reliability with high accuracy.

P-GD.3 **Impact of Forming Gas Annealing on the Degradation Dynamics of Ge-Based MOS Stacks**
F. L. Aguirre, S. M. Pazos, F. R. Palumbo, S. Fadida, R. Winter*, M. Eizenberg*, National Scientific and Technical Research Council (CONICET), UTN-CNEA* Technion-Israel Institute of Technology*

Influence of FGA on Ge based MOS is analyzed in terms of electrical stress. The FGA reduces the charge trapping for stress at negative bias, which is a common trend regardless of the HK stack. It indicates that a considerable part of the interface defects with energies close to the valence band existing in the oxide-semiconductor interface result passivated during the FGA. Ge- and InGaAs-based MOS stacks show opposite dependencies on the FGA process.

P-GD.4 **Reliability of MgO in Magnetic Tunnel Junction formed by Sputtered MgO and Oxidation of Mg**

A. Teramoto, J-I Tsuchimoto, M. Hayashi, H-W Park, K. Hashimoto, T. Suwa and S. Sugawa, Tohoku University

The film property and the breakdown characteristics of the MgO films formed by the RF sputtering of MgO and oxidation of Mg in CoFeB/MgO/CoFeB structure. The both RF-MgO and Mg oxidation film property improved by the annealing. The breakdown of the RF-MgO depends on the stress current during the constant current stress, however that of the Mg oxidation film occurs at the defect site.

P-GD.5 **Study of Dynamic TDDB in Scaled FinFET Technologies**
K. Joshi, S.W. Chang, D.S. Huang, P.J. Liao, Y.–H. Le, Taiwan Semiconductor Manufacturing Company

Impact of SHE has been studied on FinFET devices under dynamic stress. A large channel temperature increase is observed under On-State stress which leads to degradation of TDDB, however, less impact of Off-State stress. MC simulators are developed to predict Off-State, On-State and Dynamic TDDB stress. It is shown that SHE in FinFETs leads to TDDB degradation only at higher bias, however, at use conditions; SHE has little impact for both NMOS & PMOS devices.

P-GD.6 **Dielectric Breakdown in Hexagonal Boron Nitride Dielectric Stacks**
X. Liang, F. Palumbo, Y. Shi, F. Hui, B. Yuan, X. Jing and M. Lanza Martinez, Soochow University and *National Scientific and Technical Research Council (CONICET),*

Hexagonal Boron Nitride (h-BN) could be a competitive solution due to its intrinsic excellent insulating ability and good interaction with graphene and other two dimensional (2D) materials. The implementation of new materials in electronic devices requires deep analyses to predict long-term degradation. This paper presents the first device-level reliability study of h-BN dielectric stacks and the complete dielectric breakdown (BD) process.

P-GD.7 **Percolation Defect Nucleation and Growth as a Description of the Statistics of Electrical Breakdown for Gate, MEOL and BEOL Dielectrics**
Y.C. Ong, S.C. Lee and A.S. Oate, Taiwan Semiconductor Manufacturing Company

We show that gate, middle end of line (MEOL) and back end of line (BEOL) dielectrics used in advanced Si technologies exhibit a common mechanism of breakdown involving the formation (nucleation) and growth of localized percolation defects. Consequently, industry standard reliability evaluations likely significantly underestimate dielectric reliability in circuit applications.

P-GD.8 **Oxide Breakdown Path as a Nanoscale Electro-Optical Switch/Sensor**
Y. Zhou, D. S. Ang, P. S. Kalaga, and S. R. Gollu, Nanyang Technological University

Visible-light-controlled resistance switching of the oxide breakdown path is demonstrated. Two distinct digital switching behaviors pertaining to the soft and hard oxide breakdown are revealed for the first time. For soft breakdown, the leakage current is decreased when the light is turned on, and is increased when the light is turned off. For hard breakdown, it behaves oppositely. The results suggest that the breakdown path may function as a nanoscale electro-optical switch/sensor.

P-GD.9 **High Voltage Time-Dependent Dielectric Breakdown in Stacked Intermetal Dielectrics**
S. H. Shin, Y-. P. Chen, W. Ahn, H. Guo, B. Williams, J. West, T. Bonifield, D. Varghese, S. Krishnan and M. A. Alam, Purdue University

There are increasing demands on high power applications. A new multi-kV voltage transformer, which uses IC-backend intermetal dielectric as an ultra-compact capacitive voltage-divider to connect high and low

voltage ICs, is easily integrated with multi-chip IC platform. The fundamental understanding of DC, AC, and thickness-dependent dielectric breakdown of this CMP-polished, stacked PECVD dielectric, will frame its properties in the broader context of TDDB-theory of traditional dielectrics, and will encourage diversified use of the core technology.

Metallization Reliability

P-MR.1 **Electromigration Failure Rate of Redundant Via**
J.-G. Ahn, P.-C. Yeh and J. Chang, Xilinx, Inc.

We derived two methods to get Electromigration (EM) Failure Rate of redundant via (RV) by Monte Carlo (MC) simulation and analytic formulation and showed the results are identical. The two methods are applied to get a simple trend, which can be used to predict EM Failure Rate of general RV cases.

P-MR.2**Transient Self-Heating Modeling and Simulations of Back-End-of-Line Interconnects**
A. Kim, B. Li and B. Linder, IBM Systems

We present an enhanced steady-state thermal conductance model improved from the previously reported model and compact transient models that accurately predict time-dependent thermal behavior of an isolated metal carrying transient electrical signal embedded in dielectric material. Results of analytical models developed and presented in this work are in excellent agreement with those obtained by fully transient two-dimensional finite element simulations. Use of analytical models is much more advantageous over time-consuming finite element simulations.

P-MR.3 **Modeling Self-Heating Effects in advanced CMOS Nodes**
M. Arabi, X. Federspiel, A. Cros, V. Huard and C. Ndiaye, STMicroelectronics

In this paper, we analyzed the impact of the self-heating, observed on Back End of Line (BEoL) structures and NMOS transistors, in technology 28nm FDSOI. The metal characterization is required to calculate the thermal resistance (Rth). A given model relate the calculated thermal resistance to thermal conductivity (k). Rth and k are the input data used for the BEoL self-heating simulation.

Memory Reliability

P-MY.1 **Correlation between SET-State Current Level and Read-Disturb Failure Time in a Resistive Switching Memory**
P. C. Su, C. W. Wang, and Tahui Wang, National Chiao-Tung University

The relationship between SET-state current level and read-disturb failure time in a tungsten oxide RRAM is characterized and modeled. We found that read-disturb failure time is greatly improved by several orders of magnitude as SET-state current level increases a few times. We develop an analytical model to correlate read-disturb failure with SET-state current level. Our model provides a physical insight into the geometric effect of a conductive filament on read-disturb failure time.

P-MY.2 **Sub-pJ Consumption and Short Latency Time in RRAM Arrays for High Endurance Applications**
G. Sassine, C. Nail, L. Tillie, D. Alfaro Robayo, A. Levisse, C. Cagli, K. El. Hajjam, J.F. Nodin, E. Vianello, M. Bernard, G. Molas, E. Nowak. CEA, LETI, MINATEC Campus

Program operations are optimized for low power and short latency time application in RRAM kb arrays. Origin of consumption in SET and RESET operations is quantified on RRAM technology. Specific patterns are evaluated to reduce latency and energy consumption. Innovative circuit with on the fly switching detection is proposed, allowing to reduce programming consumption down to single pJ in large memory arrays.

P-MY.3 **High-Temperature and High-Field Cycling Reliability of PZT Films Embedded within 130 nm CMOS**
G. Walters, P. Chojecki, A. Garraud, S. Summerfelt, J. A. Rodriguez*, A. G. Acosta* and T. Nishida, University of Florida, *Analog Technology Development, Texas Instruments*

We present a reliability study of PZT-polarization retention after exposure to high temperatures and high-field cycling. Extraction of Preisach distribution after thermal depolarization and imprint confirms these observations: positive coercive voltage changes up to 45% while negative coercive voltage hardly changes (8%). Under accelerated aging via high electric fields (2.4V), maximum wake-up at 10^6 cycles followed by fatigue >10^8 cycles are observed. Asymmetry in coercive voltage is minimized after wake-up and remanent polarization maximized.

P-MY.4 **Suppression of Endurance-stressed Data-retention Failures of 40nm TaOx-based ReRAM**
Shouhei Fukuyama, Kazuki Maeda, Ryutaro Yasuhara, Shinpei Matsuda and Ken Takeuchi, Chuo University, *Panasonic Semiconductor Solutions Co., Ltd.*

This work investigates data-retention characteristics after different set/reset endurance cycles in ReRAM. The reliability of ReRAM depends on data-retention time in LRS, while data-retention time of HRS improves by the proposed write method "Finalize". The current distribution of LRS shifts overall to HRS side. Thus, the data-retention characteristics in LRS are determined by typical cells of the major current distribution. The physical model which is consistent with both endurance stress and data-retention characteristics are proposed.

P-MY.5 **Relaxing the STT-MRAM Reliability Challenge by Scaling MgO Thickness**
BJ O'Sullivan, S Van Beek, Ph. J. Roussel, S. Rao, W. Kim, S. Couet, J. Swerts,F. Yasin, D. Crotti, D. Linten, G. Kar, imec *also at KU Leuven,*

In this work, we detail a novel methodology to extract the magnetisation switching and breakdown characteristics from a single d.c. ramped voltage stress (RVS) measurement of STT-MRAM devices. We demonstrate how the switching and breakdown parameters are strongly interdependent for ultra-thin MgO layers. We validate this methodology by successfully correlating our results with the more widely reported pulsed-breakdown results.

P-MY.6 **Chip-Level Characterization and RTN-Induced Error Mitigation Beyond 20nm Floating Gate Flash Memory**
T. W. Lin, S.H. Ku, C.H. Cheng, C.W. Lee, J.-H., W.-J. Tsai, T.C. Lu, W.P. Lu, K.C. Chen, T. Wang, and C.-Y. Lu, Macronix International Co.

Vt instability caused by giant RTN in floating-gate flash memories in 1xnm is studied. Experiments reveal that the RTN would cause a tail which re-distributes to a "Gaussian-shape" rapidly and was measured by the product tester. A Multi-Times Verify (MTV) method to mitigate the tail is also exhibited. Further, a probability model to portray the compact Vt distribution under MTV is proposed. The impact of MTV on the reduction of Error-correcting-code bit is also demonstrated.

P-MY.7 **Cross Error Elimination ECC by Horizontal Error Detection and Vertical-LDPC ECC to Increase Data-Retention Time by 230% and Acceptable Bit-Error Rate by 90% for 3D-NAND Flash SSDs**
S. Suzuki, Y. Deguchi, T. Nakamura, K. Mizoguchi and K. Takeuchi, Chuo University,

XEE ECC with HED and V-LDPC is proposed to extend the data-retention lifetime of 3D-TLC NAND flash. HED improves the error correction capability of LDPC by evaluating the error bits in the horizontal direction. Moreover, V-LDPC improves the worst reliability in each WL in the vertical direction. This paper investigates the reliability of 3D-TLC NAND flash by XEE ECC. As a result, the data-retention lifetime and acceptable BER are extended by 230% and 90%, respectively.

Process Integration

P-PI.1 **Investigation of Monolayer MX_2 as Sub-Nanometer Copper Diffusion Barriers**
Kirby Smithe, Zhongwei Zhu, Connor Bailey, Eric Pop* and Alex Yoon, Lam Research Corp., *Stanford University*

We investigate four monolayer materials – MoS_2, WS_2, $MoSe_2$, and WSe_2 – on Si as possible sub-nm Cu diffusion barriers. SEM and TEM images suggest that W-based TMDs act as barriers up to 360°C, while Mo-based TMDs fail as low as 300°C. SEM indicates failure occurs as pinholes, suggesting mechanical damage may be the origin of failure. Further analysis by XPS on as-grown TMDs indicates that directly-grown TMDs still have potential as sub-nm diffusion barriers.***Product Reliability***

P-PR.1 **Evaluation on Flip-flop Physical Unclonable Functions in a 14/16-nm Bulk FinFET Technology**
H. Zhang, H. Jiang, M.R. Eaker, K.J. Lezon, B. Narasimham, N.N. Mahatme**, L.W. Massengill, B.L. Bhuva, Vanderbilt University, Nashville TN 37212, 2Broadcom Corporation*

Physical unclonable functions (PUF) has been used to securely authenticate devices in electronic systems. In this paper, different flip-flop (FF) designs at a 14/16-nm bulk FinFET technology node have been evaluated for suitability as PUF generator. Randomness, repeatability and uniqueness is considered to rank order different FF designs. FF-based PUFs using reduced supply voltage are seen to be more promising compared to those for nominal supply voltages.

Photovoltaics

P-PV.1 **Charge State Evaluation of Passivation Layers for Silicon Solar Cells by Scanning Nonlinear Dielectric Microscopy**
*K. Kakikawa, Y. Yamagishi, K. Tanahash*i, H. Takato* and Y. Cho, Tohoku University, *National Institute of Advanced Industrial Science and Technology*

Nano scale charge states in Al3O3 passivation layers of Si solar cells and at Al3O3/Si interface were evaluated by using scanning nonlinear dielectric microscopy. The inhomogeneous distribution of fixed charge Qox in Al3O3 thin film and interface density of sate Dit was observed. Variations of Qox and Dit caused by annealing were clearly detected. Moreover, increase of negative fixed charge density by annealing was quantitatively evaluated.

P-PV.2 **Performance Improvement of Tandem Amorphous / Microcrystalline Si Photovoltaic Modules under Changes in Illumination Conditions**

*F. Ricco Galluzzo, A. Scuto, C. Gerardi 3, A. Battaglia4, A. Canino***, F. Aleo 3 and S. Lombardo, CNR IMM, *Università degli Studi di Catania, **ENEL Green Power, ***3SUN S.r.l.*

The Staebler and Wronski light soaking effect in a-Si:H implies a solar cell performances worsening. Previous our stress tests indoor on a-Si:H and tandem solar cells have proved that under suitable conditions an improvement of the cell perfomances is possible. In this work, we report on stress tests outdoor on commercial tandem amorphous/microcrystalline Silicon devices, highlighting the improvements of their electrical performances in the afternoon. Possible causes of such effect are discussed.

Reliability Testing

P-RT.1 **Effect of HCI Degradation on the Variability of MOSFETS**
C. Zhou, K.A. Jenkins, P.I. Chuang and C. Vezyrtzis, IBM T.J. Watson Research Center

The effect of HCI (hot-carrier injection) degradation on the variability of FETs is studied with a novel test structure. Using a space- and time-efficient technique, a large number of degradation measurements can be taken in the time usually used for a single device. Studies with this circuit have shown that variability of 14nm finFETs is actually reduced by the degradation caused by HCI stress.

P-RT.2 **Temperature and Voltage Effects on HTRB and HTGB Stresses for AlGaN/GaN HEMTs**
O. Chihani, L. Theolier, A. Benssousan, J.-Y. Deletage, A. Durier* and E. Woirgard, Univ. Bordeaux, CNRS, *2 IRT Saint-Exupery*

We investigate the degradation of AlGaN/GaN HEMTs submitted to HTRB and HTGB step-stresses. Steps in terms of temperature and voltage were done in order to distinguish the effect of each stressor. The main aim is to establish a lifetime model taking account multiple degradation mechanisms for a large range of temperature and voltage. The experiments evidenced two failure rate mechanisms that are activated simultaneously within the range of temperature and voltages selected.

P-RT.3 **Interaction of Permeats During the Measurement of Permeation Coefficients of Dense Polymer Films Under Realistic Conditions**
A. Piekarczyk, X. Xu, M. Köhl, K.-A. Weiß, Fraunhofer Institute for Solar Energy Systems ISE

In this publication the simultaneous measurement of several permeates are analyzed showing the interdependence of permeation rates of three major permeates (water vapor, oxygen and nitrogen gas) depending on their concentration. Based on these results the measurements of the permeability for single permeates can only be seen as an approximation by ignoring competitive effects of different permeates as found for most application environments, like in photovoltatics.

P-RT.4 **Polysilicon Resistor Stability Under Voltage Stress for Safe-Operating Area Characterization**
C. Kendrick, M. Cook, J. Gambino, T. Myers, J. Slezak and Y. Watanabe, ON Semiconductor

High resistance polysilicon resistors have been characterized by DC and pulsed I-V measurements over temperature, and DC and pulsed voltage stress/measurement cycling. The combination of these measurements along with resistor linearity and electromigration are used to determine the maximum safe-operating area. It is shown that the resistance shifts at high current conditions cannot be explained by electromigration alone, and are instead attributed to changes in the g polysilicon resistor itself.

P-RT.5 **Reliability Characteriscs of MIM Capacitor Studied Using ΔC-F Characteristics**
S. C. Kang, S. K. Lee, S. Heo, S. M. Kim, S. K. Lim and B. H. Lee, Gwanju Institute of Science and Technology

We propose a simple monitoring method for the quality of MIM capacitor. The differences in the slope of C-F curve at low and high frequency are found to be a good indicator showing the difference in the reliability characteristics of MIM capacitor. Asymmetric interface trap generation near top or bottom electrode could be monitored and clear difference was observed at various dielectric thicknesses, measurement temperature and stack structures.

Soft Error

P-SE.1 **Investigation of Alpha-Induced Single Event Transient (SET) in 10 nm FinFET Logic Circuit**
T. Uemura, S. Lee, D. Min, I. Moon, J. Lim, S. Lee, and S. Pae, Samsung Electronics

This paper investigates alpha-induced single event transient (SET) in combinational-logic in 10 nm bulk FinFET technology. FinFET technology improves SET in combinational-logic as well as single event upset (SEU) in flip-flops. However, the improving ratio in SET is ten times smaller than that in SEU. As a result, SET ratio to SEU in 10 nm FinFET technology is higher than that in bulk planer technologies.

P-SE.2 **Study of TID Effects on One Row Hammering using Gamma in DDR4 SDRAMs**
D. Yun, M. Park, C. Lim and S. Baeg, University of Hanyang

The Total Ionizing Dose (TID) effects on DDR4 SDRAM were investigated using Co60 γ-rays. While degradation in retention time was observed, no retention error was observed at a retention time of 64-ms in 80 ℃ and 90 krad exposure. Unlike that in retention time degradation, significant degradation in one row hammering threshold was observed. The threshold was reduced by up to 153 k, which is a 218 % reduction when compared to pre-radiation values.

P-SE.3 **Sensitivity to Soft Errors of NMOS and PMOS Transistors Evaluated by Latches with Stacking Structures in a 65 nm FDSOI Process**
K. Yamada, H. Maruoka, J. Furuta and K. Kobayashi, Kyoto Institute of Technology

Three different latch structures are fabricated in a 65 nm FDSOI process.We evaluate soft-error tolerance of latches by device simulations and α particle, neutron irradiation tests in order to identify which transistor type is dominant to cause soft errors. The latch structure including an inverter with stacked NMOS and unstacked PMOS transistors has enough tolerance against soft errors. It suggests that soft errors are dominant on NMOS transistors in the terrestrial region.

P-SE.5 **Design Soft-Error-Aware Circuits with Power and Speed Optimization**
H. Jiang, H. Zhang, B. Narasimham, L. W. Massengill, and B. L. Bhuva, Vanderbilt University, *Broadcom Corp.*

Even though power consumption for ICs has emerged as the most constraining aspect, it is important to deliver circuit designs that also meet area, speed, and SER specifications. DFF designs with different threshold voltages are fabricated at the 14/16-nm bulk FinFET CMOS technology node and evaluated for speed and SER from a power perspective. The results are used to create a model that will allow designers to identify optimum design and operating parameters to meet multiple design constraints.

P-SE.6 **Single-Event Effects on Optical Transceiver**
K. J. Lezon, S.-J. Wen, Y.-F. Dan*, R. Wong*, B. L. Bhuva, Vanderbilt University, *Cisco Systems*

All communications systems use optical modules to achieve data transfer speeds in 10's of GHz range. With increasing reliance on communication systems, the impact of soft errors in optical transceiver modules

has become a primary concern for system performance. This paper examines neutron-induced soft-error rates and associated failure modes of optical transceivers.

System Reliability

P-SR.1 **Weibull Cumulative Distribution Function (CDF) Analysis with Life Expectancy Endurance Test Result of Power Window Switch**
M. Lee, J. Kim, D. Lim, and D. Cho, LS Automotive

The first goal of this task is to develop realistic worst case lifetime endurance test specification because existing large number of switch test standards cannot induce degradation mechanism which makes the switches less reliable. 2nd goal is to assess quantitative reliability status of PWS based on test specification newly developed thru this project and to develop how to improve product reliability based on PWS degradation mechanisms.

P-SR.2 **Development of a Flexible Wearable Biometric Band and Smartphone Application for Remote User-Monitoring**
A. Pradeep Lall, B. Hao Zhang, C. Rahul Lall, Auburn University, * Stanford University*

Reducing paramedic response times to five minutes could nearly double survival rates of patients experiencing life-threatening medical conditions. Maintenance of an independent lifestyle with a comparable level of monitoring requires the development of devices which can provide continuous monitoring and timely medical intervention when needed, without the tie-down constraints of a hospital setting. In this project, a novel rapid-response flexible wearable bioelectronics device has been developed.

Transistors/Beyond CMOS

P-TX.1 **Low Frequency Noise in MoS_2 Negative Capacitance Field-effect Transistor**
S. Alghamdi, M. Si, L. Yang and P.D. Ye, Purdue University

We report for the first time on low frequency noise studies in MoS2 NC-FETs. The low frequency noise is found to decrease with thicker ferroelectric HZO, in contrast to the conventional high-k MOSFETs, the negative capacitance concept of the ferroelectric HZO practically explains the noise measurement results.The key result is that the negative capacitance can not only improve the device on- and off-state performance, but can also suppress the noise.

P-TX.2 **Hot Carrier Effects on the RF performance Degradation of Nanoscale LNA SOI nFETs**
D.P. Ioannou, Y. Tan, R. Logan, K. Bandy, R. Achanta, P.C. Wang, D. Brochu and M. Jaffe GLOBALFOUNDRIES

We report on the hot carrier effects on the DC and small signal RF parameters of nanoscale SOI nMOSFETs developed for high performance low noise amplifier circuits. This is the first study done on SOI nFETs scaled down to 35 nm where stress experiments specifically designed to address the LNA operational bias conditions and RF figures-of-merits are carried out. The obtained results lay the foundation for a reliability-aware RF LNA design.

P-TX.3 **Hot Carrier Induced TDDB in HV MOS: Lifetime Model and Extrapolation to Use Conditions**
G. Sasse, NXP Semiconductors

In this paper we report on a lifetime extrapolation model for hot carrier induced time dependent dielectric breakdown in HV MOS devices. The proposed lifetime model is based on findings from literature, supplemented with new experimental data on several types of HV pMOS devices. Furthermore the methodology to make accurate lifetime extrapolations towards use conditions is discussed.

P-TX.4 **Key Parameters Driving Transistor Degradation in Advanced Strained SiGe Channels**
*V. Huard, C. Ndiaye, M. Arabi, N. Parihar** X. Federspiel, S. Mhira, S. Mahapatra** and A. Bravaix**
STMicroelectronics, *ISEN-REER, IM2NP, ** IIT Bombay*

The paper proposes new physical explanations to explain the impact of compressive strain, germanium content and nitrogen content on NBTI and HCI degradation on pMOS transistors. Both compressive strain and Ge content impact on NBTI degradation is found to relate to modifications in band structure of channel. Excellent agreement between theory and experimental results shed new light on NBTI degradation mechanism and the physics lying behind. HCI degradation is well explained by recent energy-driven theory.

P-TX.5 **Prediction of NBTI Stress and Recovery Time Kinetics in Si Capped SiGe p-MOSFETs**
N. Parihar and S. Mahapatra, IIT Bombay

Measured NBTI stress and recovery temporal kinetics at different experimental conditions are predicted in Si and SiGe p-MOSFETs. Mutually uncorrelated contributions from interface and bulk trap generation and hole trapping in pre-existing bulk traps are used to predict the overall threshold voltage shift. Process variations such as Si cap and quantum well thickness and Ge% in QW and their impact on stress-recovery kinetics are modeled.

P-TX.6 **Investigation on the Amplitude Coupling Effect of Random Telegraph Noise (RTN) in Nanoscale FinFETs**
S. Guo, Z. Lin, R. Wang, Z. Zhang, Z. Zhang, Y. Wang and R. Huang, Peking University

Based on the complex RTN data in FinFETs, the impacts of the trap coupling effect are studied statistically. The coupling effect is found to be enhanced by the double-side coupling mechanism in FinFETs. The non-monotonic VG dependence of amplitude coupling strength is observed, which is contributed by the evolution of channel percolation paths. In addition, the impacts of stress on the coupling strength are studied. The impacts of amplitude coupling on circuits are also investigated.

P-TX.7 **PBTI Evaluation of $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ Nanowire FETs with Al_2O_3 and $LaAlO_3$ Gate Dielectrics**
Y. Li, K. L. Wang, S. Y. Di, P. Huang, G. Du and X. Y. Liu, Institute of Microelectronics, Peking University

This paper investigates the PBTI of InGaAs nanowire FETs with different channel and gate dielectrics by 3D-Kenetic Monte Carlo method. It is found that indium and gallium components of channel impact on PBTI, and there is worse PBTI with larger In component. Moreover, PBTI along nanowire thickness (TNW) and width (WNW) directions shows different due to non-uniform electrical field. With sandwich structure channel, the Vth shift difference of TNW/WNW can be enlarged in high temperature.

P-TX.8 **Interface Engineering of Ferroelectric Negative Capacitance FET for Hysteresis-Free Switch and Reliability Improvement**
*C-C Fan, C-H Cheng, C. Liu, C-Y Tu, G-L Liou and C-Y Chang, National Chiao-Tung University and *National Taiwan Normal University*

In this work, we successfully achieve a hysteresis-free NCFETs by exploiting a defect passivation scheme and simultaneously provide a new insight into the gate-oxide reliability of NCFET. The fluorine-passivated HfAlOx NCFET features a sub-30-mV/dec, a negligible hysteresis-free switch of ~10mV and >1E7 Ion/Ioff ratio. Most importantly, fluorine passivation effectively suppress the generation of shallow traps during stress to maintain NC operation and SILC immunity, which has been verified by transient pulse IV measurement.

Wide Band Gap/Compound/Optoelectronics

P-WB.1 **Threshold Voltage Shift and Interface/Border Trapping Mechanism in Al_2O_3/AlGaN/GaN MOS-HEMTs**
J. Zhu, B. Hou, L. Chen, Q. Zhu, L. Yang, M. Mi, X. Zhou, P. Zhang, X. Ma and Y. Hao, Xidian University

Trap states and the induced voltage shift in Al2O3/ AlGaN/GaN MOS-HEMTs were studied. Interface trapping is found dominant at low gate voltage, and then border trapping become remarkable with voltage above 5 V due to the extra trapping energy. At low field, border de-trapping has a very long emission time constant, resulting in the maintainable voltage shift; while Vth recovery can be achieved after "breakdown" due to the tunneling de-trapping mechanism at high field.

P-WB.2 **Investigation of the Pulsed-IV Degradation Mechanism of GaN-HEMT under High Temperature Storage Tests**
Y. Kurachi, Y. Tateno, T. Yonemura, M. Furukawa*, H. Yamamoto, Y. Nose and S. Shimizu, Sumitomo Electric Device Innovations, Inc., *Sumitomo Electric Industries, Ltd.*

The purpose of this study is to investigate the physical mechanism of pulsed-IV degradation under high temperature storage tests. Using the measurements of the pulsed S-parameters immediately after the voltage stress was applied, we carried out the delay analysis. As a result, we found that the so-called "virtual gate" region extended toward the drain electrode due to high temperature storage, and we concluded that the electron tunnel injection probability increased and degraded the pulsed-IV characteristics.

P-WB.3 **Failure Mode Analysis of GaN-HEMT Under High Temperature Operation**
Y. Tateno, Y. Kurachi, H. Yamamoto* and T. Nakabayashi, Sumitomo Electric Industries, Ltd., *Sumitomo Electric Device Innovations, Inc.*

The purpose of this study is to investigate the physical mechanism of the threshold voltage shift of GaN-HEMT in high temperature storage tests. Using microscopic Raman spectrometry, we found the crystal extends vertically. From this observation, we concluded that one possible reason for the threshold voltage shift in high temperature storage tests is the change of the piezopolarization density dependent on the change of the crystal distortion under the gate metal.

P-WB.4 **A Novel GaN HEMT Degradation Mechanism Observed During HTST Test**
F. Iucolano, A. Parisi, S. Reina, and A. Chini, STMicroelectronics, *University of Modena and Reggio Emilia*

The Imax current reduction after high temperature short term tests in RF-GaN HEMT was investigated. A "critical-voltage" like degradation was observed with voltage levels correlated with the pinch-off voltage of the MIS structure. The recoverable nature of the phenomena and the positive temperature dependence of both the IMAX reduction and leakage currents within the passivation layer allowed us to propose a novel interpretation based on a charge-injection process from the FP into SiN/AlGaN.

P-WB.5 **Investigation of Degradation Phenomena in GaN-on-Si Power MIS-HEMTs under Source Current and Drain Bias Stresses**
C .Y. Yang, T. L. Wu, T. E. Hsieh and E. Y. Chang, National Chiao-Tung University

We investigate the degradation phenomena in GaN-on-Si MIS-HEMTs in the cascode topography for E-mode power switching applications. Different stress conditions are used to investigate the IS and VD dependent degradation. There are two results from findings. One is the phenomena under a low VD stress, the other is a different degradation phenomena under high VD stress. We also show the difference from different IS induced. The conclusion is instability degradation is mainly triggered by VD.

Session 6A - FOCUS SESSION: To Space and Beyond: Methods and Themes to Develop Reliable Systems!

Session Chairs: *Guneet Sethi, Amazon Lab 126, Rob Kwasnick, Intel*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6A.1 **Automotive Functional Safety (Invited)**
R. Mariani, Intel

8:30 AM
6A.2 **Making the Connection Between Physics of Failure and System-level Reliability for Medical Devices (Invited)**
A. Fenner, Medtronic

8:55 AM
6A.3 **Key Attributes to Achieving 99.999+ Satellite Availability (Invited)**
B. Kosinski, Space Systems/Loral, LLC

9:20 AM
6A.4 **Comprehensive Process of Quality and Reliability for Organic Light Emitting Diode Applied Flexible Mobile Display (Invited)**
J. Park, Samsung

9:45 AM
6A.5 **Prognostics and Health Monitoring of Electronic Systems: A Reliability-Physics Approach (Invited)**

P. Lall, Auburn University

Session 6B - Failure Analysis

Session Chairs: *Kevin Johnson, Intel, Baohua Niu, TSMC*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6B.1 **Solving Critical Issues in 10nm Technology using Innovative Laser-based Fault Isolation and DFT Diagnosis Techniques**
L. Zaren Endrinal, R. Kinger, L. Ranganathan and A. Sheth, Qualcomm Technologies, Inc.

This paper will present an innovative technique in performing fault isolation in our latest 10nm product to resolve 35% yield loss issue due to stuck-at-fault (SAF) logic failures during first silicon bring up. The main issue was the lack of viable diagnostic results, which made this problem almost impossible to solve. With the use of special DFT and new fault isolation techniques, we were able to crack the case and find the root cause.

8:30 AM
6B.2 **Cathodoluminescence Spectroscopy for Failure Analysis and Process Development of GaN-Based Microelectronic Devices (Invited)**
C. Monachon, Attolight

8:55 AM
6B.3 **Electrical Method to Localize the High-Resistance of Nanoscale CoSi2 Word-Line for OTP Memories**
M.-Yi Lee, T.-Y. Chang, W.-F. Hsueh, L.-K. Kuo, D.-J. Lin, Y.-H. Chao, U. J. Tzeng and C. Y. Lu, Macronix International Co.

The defective high-resistance in a nanoscale Cobalt silicide (CoSi2) word-line (WL) was observed for a high density of non-volatile memory. An electrical method through analyzing the variation of threshold voltage of memory cells with its physical position is proposed to help the localization of defective position, identify the root cause of CoSi2 agglomeration, and also provide a method to detect this kind of defective WL.

9:20 AM
6B.4 **Estimating Transistor Channel Temperature using Time-Resolved and Time-integrated NIR Photoemission (Invited)**
F. Stellari, IBM

9:45 AM
6B.5 **BEOL TDDB Reliability Modeling and Lifetime Prediction Using Critical Energy to Breakdown**
*P. S.Chen, S.C. Lee[*], A. S. Oates[*], and C. W. Liu[**], National Taiwan University, *Taiwan Semiconductor Manufacturing Company, **National Nano Device Laboratories*

By combining modeling of the leakage current of BEOL capacitors with TDDB data, we show that the hard breakdown of capacitors during electrical stress is related to the leakage current flowing through the dielectric. Moreover, we find the breakdown occurs after a critical energy density has been dissipated in the dielectric. We find that the tunneling currents do not contribute to the breakdown due to the absence of anode hole injection for the metal-insulator-metal structure.

Session 6C - Photovoltaics Reliability

Session Chairs: *Michael Daenen, Hasselt University, Karl-Anders Weiss, Fraunhofer - ISE*
Thursday, March 15

8:00 AM - Session Introduction

8:05 AM
6C.1 **Permanent shunting from passing shadows: Reverse-bias damage in thin-film photovoltaic modules (Invited)**
T. Silverman, NREL

8:30 AM
6C.2 **Modified Transformerless Dual Buck Inverter with Improved Lifetime for PV Applications**
A. Khan, L. Ben-Brahim, A. Gastli, Department of Electrical Engineering, Qatar University

Single-Phase grid-tied Photovoltaic (PV) inverter's reliability is severely deteriorated by the double grid frequency power pulsation, since this pulsation requires large unreliable DC-Link capacitors installation. Therefore, a modified Dual-Buck-Inverter (DBI) topology and control is proposed. The proposed modification allows utilizing the Common-Mode (CM) operation of the inverter to perform Active-Power-Decoupling (APD). Finally, the analyses were validated on a 3kW prototype and showed that a 30uF capacitor is adequate to achieve a ripple free DC-Bus voltage.

8:55 AM
6C.3 **Evaluation of the Silicon, Organic, and Perovskite Solar Cell Reliability with Low-frequency Noise Spectroscopy**
G. Landi, C. Barone, C. Mauro, S. Pagano and H. C. Neitzert, Università di Salerno

Low-frequency noise spectroscopy has been used to monitor electronic properties of solar cells under temperature or radiation stress. For all the investigated cells, the low-frequency noise analysis evidences a clear correlation of the recombination and the transport processes with the device performances.

9:20 AM
6C.4 **Mechanical and chemical adhesion at the encapsulant interfaces during the lamination of photovoltaic modules**
P. Nivelle, T.Borgers, E. Voroshazi*, J. Poortmans*, J. D'Haen, W. De Ceuninck, and M. Daenen, Hasselt University, *imec,*

This work investigates the influence of the flux use on the adhesion strengthof encapsulants to the metallization/interconnection of a photovoltaic module as it can have a major effect on the long term reliability. In short, the influence of flux is predominantly determined by the encapsulant type. The differences measured in adhesion strength could be correlated to a difference in macro-scale roughness at the interface and in the quantity of solder particles present.

9:45 AM
6C.5 **A New Mechanism of Signal Path Charging Damage Across Separated Power Domain Deep N-Well Interface (Late News)**
Y.-L. Chu, TSMC

A new damage mechanism of cross domain interface from the non-DNW to DNW region is observed, which can be observed inside DNW. In addition, both NMOS and PMOS transistors are damaged instead of NMOS only. This new damage mechanism model is characterized and verified using test patterns in a 40nm logic process together with SPICE simulation results. Several prevention solutions to eliminate the charging damage are proposed and verified.

Session 6D - Memory Reliability

Session Chairs: *Alessandro Spinelli, Politecnico di Milano, Andrea Chimenton, Intel*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM
6D.1 **Investigation of Data Pattern Effects on Nitride Charge Lateral Migration in a Charge Trap Flash Memory by Using a Random Telegraph Signal Method**
Y. H. Liu, H. Y. Lin, Tahui Wang, W. J. Tsai, T. C. Lu*, K. C. Chen*, and Chih-Yuan Lu*, Dept. of Electronics Engineering, National Chiao-Tung University, *Macronix International Company Ltd.,*

Data charge pattern effects on nitride charge lateral migration and Vt retention loss in a charge trap flash memory is investigated by using an random telegraph signal method. We find that trapped hole lateral movement is dependent on the program Vt level of a neighboring bit through the modification of a built-in electric field. At a similar nitride electric field, trapped holes are found to be more mobile than trapped electrons in lateral migration.

11:00 AM
6D.2 **Impact of Specific Failure Mechanisms on Endurance Improvement for HfO2-based Ferroelectric Tunnel Junction Memory**
M. Yamaguchi, S. Fujii, Y. Kamimuta, S. Kabuyanagi, T. Ino, Y. Nakasaki, R. Takaishi, R. Ichihara, M. Saitoh, Toshiba Corporation

We conducted a detailed investigation on failure mechanisms for the HfO2 FTJ during set/reset cycling endurance by combining methodology of the well-known reliability evaluation (TDDB) and the memory-specific evaluation. As a consequence, we clarify the failure mechanism and successfully demonstrate a way to improve cycling endurance. Based on these findings, a potential cycling endurance over 10^6 cycles is shown to be expected, implying the HfO2 FTJ has a high potential for future non-volatile memory applications.

11:25 AM
6D.3 **Investigation of the Endurance of FE-HfO2 Devices by Means of TDDB Studies**
K. Florent, A. Subirats, S. Lavizzari*, R. Degraeve*, U. Celano*, B. Kaczer*, L. Di Piazza*, M. Popovici*, G. Groeseneken and J. Van Houdt, KU Leuven, *imec*

Ferroelectric HfO2 devices are potential candidates for non-volatile memory applications. However they often exhibit a pinched hysteresis, which requires the application of cycles to “wake-up” the device. In this paper, endurance of FE-Al:HfO2 MIM is investigated using TDDB measurements. An improvement in TDDB lifetime is observed with cycling. A hypothesis involving rearrangement of defects is proposed to explain this behavior.

1:10 PM
6D.4 **Carbon Electrode in Ge-Se-Sb Based OTS Selector for Ultra Low Leakage Current and Outstanding Endurance**
A. Verdy, G. Navarro, M. Bernard, S. Chevalliez, N. Castellani, E. Nolot, J. Garrione, P. Noé, G. Bourgeois, V. Sousa, M.-C. Cyrille and E. Nowak, CEA, LETI, MINATEC Campus

In this paper we study the reliability of a Ge-Se-Sb based OTS Selector. We highlighted that the Ti diffusion from the electrode appears to be the main mechanism responsible for the degradation of the device performances. We engineered a thin carbon layer as electrode, achieving an ultra-low leakage current lower than 10 pA and an endurance of 1G cycles. These results are among the best reported so far for an OTS selector technology.

1:35 PM
6D.5 **Reliability Benefits of a Metallic Liner in Confined PCM**
*W. Kim, Y. Xie**, Y. Kim**, T. Masuda*, S. Kim, R. Bruce, F. Carta, G. Fraczak, A. Ray, K. Suu*, C. Lam, M. BrightSky, J. J. Cha**, and Y. Zhu, IBM T. J. Watson Research Center, *ULVAC, Inc., **Yale University*

We demonstrate outstanding drift mitigation and void elimination as reliability benefits of a thin metallic liner. By tuning the resistivity of the liner, the confined PCM with a metallic liner yields an extremely low R-drift coefficient. We also show for the first time that confined PCM could have a self-recovering property by incorporating a metallic liner. The in-situ TEM results exhibit the robustness of the confined PCM that can recover by itself by void elimination.

2:00 PM
6D.6 **Area and Pulse Width Dependence of Bipolar TDDB in MgO STTRAM**
J. H. Lim, N. Raghavan, S.Mei, V.Naik,J.H. Kwon*, K.H. Lee*, K.L. Pey, Singapore University of Technology and Design (SUTD), *GLOBALFOUNDRIES*

Results from the bipolar pulsed endurance test reveal that the breakdown voltage is dependent on the pulse width for a given applied voltage and area of MgO. Devices with lower pulse widths for the same overall stress duration have longer lifetime due to the self-heating effects that take a few microseconds to reach the saturation temperature. We prove that self-heating effects play a more dominant role than extrinsic etch damage effects in our samples.

2:25 PM
6D.7 **The First Observation of p-type Electromigration Failure in Full Ruthenium Interconnects (Late News)**
S. Beyne, S. Dutta, O. Varela Pedreira, N. Bosman*, C. Adelmann*, I. De Wolf, Z. Tokei* and K. Croes*, KU Leuven, *imec*

We show the first electromigration (EM) failures of full ruthenium interconnects with a cross sectional area of 60nm2. The void is observed at the anode, which demonstrates that in p-type metals, such as Ru, the electromigration force acts in the direction of the electric field. The conventional representation of electromigration as electrons transferring their momentum onto the metal ions, thus has to be adapted for such metals.

Session 6E - Reliability Testing

Session Chairs: *Kevin Manning, Analog Devices, Derek Slottke, Intel*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM
6E.1 **Lateral Profiling of HCI Induced Damage in Ultra-Scaled FinFET Devices with Id-Vd Characteristics**

M. Wang, R. G. Southwick, J. H Stathis and K. Cheng, IBM Research Division, T.J. Watson Research Center

In this work, we present an experimental method to obtain the location of the pinch-off point in a MOSFET biased in saturation. The proposed methodology enables lateral profiling of hot carrier induced defects directly from measured data without the need of extensive simulation or complicated analytical modeling.

11:00 AM

6E.2 **Ambient temperature and layout impact on self-heating characterization in FinFET devices**

P. Paliwoda, Z. Chbili, A. Kerber, D. Singh, D. Misra, GLOBALFOUNDRIES Inc., *New Jersey Institute of Technology*

Self-Heating effects are going to be increasingly significant in future nodes. Understanding self-heating measurement results is of vital importance. In this paper we show for the first time through measurement that the ambient temperature can affect self-heating measurement by up to 69%. Through a series of measurements at different temperatures and dissipated power, we show that the Si fin has a more dominant effect in heat transport and its varying thermal conductivity should be accounted.

11:25 AM

6E.3 **A New Method For Quickly Evaluating Reversible and Permanent Components of the BTI Degradation**

X. Garros, A. Subirats, C. Diouf, X. Federspiel*, V. Huard*, M. Rafik*, G. Reimbold, B. Gaillard, CEA-Leti, *ST Microelectronics*

A new method denoted SRP is proposed for a quick evaluation of the reversible and permanent NBTI components responsible for NBTI degradation. The technique which can be seen as a mathematical trick is useful for a fast comparison of process leverages impacting BTI. It can also provide a simple analytical compact model suitable for SPICE-like simulator.

1:10 PM

6E.4 **Threshold Voltage Bitmap Analysis Methodology: Application to a 512kB 40nm Flash Memory Testchip**

T. Kempf, V. Della Marca, L. Baron, F. Maugain, F. La Rosa, S.Niel, A. Regnier, J.-M. Portal*, P. Masson**, STMicroelectronics, *IM2NP, **EpOC / Nice Sophia-Antipolis University*

To answer demanding reliability requirements, the Flash memory technology development needs test chips to allow large statistical studies and a product-like approach. The use of such test chips must be carefully studied to separate peripheral effect on memory reliability, and to extract electrical parameters such as threshold voltage. In this abstract, we present a methodology of bitmap analysis to extract intrinsic and extrinsic parameters during reliability test of a 512kB Flash memory test chip.

1:35 PM

6E.5 **BVDSS (drain to source breakdown voltage) instability in shield gate trench power MOSFETs**

J. Hao, A. Ghosh, M. Rinehimer, J. Yedinak, M. A. Alam, ON Semiconductor, *Purdue University,*

We develop a constant current avalanche injection stress to test BVDSS instability in charge balance power MOSFETs. Our data shows this test is very sensitive to the BVDSS instability but HTRB (high temperature reverse bias) is not. We explain why this test is more sensitive than HTRB for BVDSS instability in charge balance MOSFETs. Furthermore, we show that during constant current stress, holes are injected into the shield oxide which results in the BVDSS instability.

2:00 PM
6E.6 **Effect of Measurement Speed (µs-800 ps) on The Characterization of Reliability Behaviors for FDSOI nMOSFETs**
*Y. Qu, R. Cheng, W. Liu, J. Li, B.Y. Nguyen**, O. Faynot***, N. Xu*, B. Chen, Y. Zhao, Zhejiang University, *University of California, **Soitec, Austin, ***CEA-Leti Minatec*

We experimentally investigate the impact of measurement speed (µs-800 ps) on the characterization of reliability behaviors, HCI and PBTI, for FDSOI nMOSFETs. The results show that, due to the severe self-heating effect (SHE) in the transistors, the I-V measurement speed could significantly affect the characterization of threshold voltage (VTH) shift and drain current (IDSAT) degradation after HCI and PBTI stress. Due to the inevitable SHE in the transistor channel caused by the long measurement time.

2:25 PM
6E.7 **Non-Poissonian Behavior of Hot Carrier Degradation Induced Variability in MOSFETs (Late News)**
R. Bottini, A. Ghetti, S. Vigano, M. G. Valentini, P. Murali, C. Mouli, Micron Technology Inc.

Previously, it was reported that Hot Carrier induced MOSFET Vth shift follows a Poissonian behavior. Here, we show new data deviating from this behavior. First, in the initial stage of the HC stress, Vth shift may exhibit a super-poissonian behavior. Second, for very high stress levels, HC Vth shift standard deviation tends to saturate to a maximum value. A new physical model able to explain these phenomena is proposed and validated with numerical simulations.

Session 6F - CMOS Process Integration session

Session Chairs: *Xavier Garros, CEA, Barry Linder, IBM*
Thursday, March 15

10:30 AM - Session Introduction

10:35 AM
6F.2 **Understanding Gate Metal Work Function (mWF) impact on Device Reliability - A Holistic Approach**
P. Srinivasan, R. Ranjan, S. Cimino, A. Zainuddin, B. Kannan, L. Pantisano, I. Mahmud, G. Dilliway, T. Nigam, GLOBALFOUNDRIES Inc.

The effect on device reliability due to gate metal work function (mWF) in thin and thick gate oxide FinFETs. Lower BTI is noticed for increasing WFM1 thickness for thin oxide nFETs. Higher degradation is seen for thin and thick oxide pFETs. A dual behavior is noticed for pFETs. For TDDB, t63% increases with increasing VT caused by modulation in WFM1 thickness. A physical model ispro posed which explains the observed reliability behavior.

11:00 AM
6F.3 **Performance & Reliability of 3D Architectures (Pifet, Finfet, Omegafet)**
A. Laurent X. Garros, S. Barraud, J. Pelloux-Prayer, M. Cassé, X. Federspiel, D. Roy*, E. Vincent*, G. Ghibaudo**, F. Gaillard, CEA-LETI, *STMicroelectronics, **IMEP-LAHC, Minatec/INPG*

The impact of 3D architectures and boosters on the trade-off performance/reliability is deeply investigated in this paper. “Finfet” transistor presents a slight superior trade-off than square shaped “ΠIfet” device because of little improved performance and similar BTI&HC reliability. “Ωfet” also offers a better compromise than ΠIfet due to improved BTI reliability. Finally strained SOI & SiGeOI devices are highly suitable since they allow boosting the transistor performance without any reliability penalty.

11:25 AM

6F.4 **Reliability Studies of a 10nm High-performance and Low-power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG**

A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, S. Ramey, Intel Corporation

Development of an industry leading 10nm CMOS process technology with the highest reported drive currents and cell densities involved numerous enabling innovations, judicious choice of design rules, novel features, and most importantly a relentless pursuit of process-reliability co-optimization. This paper elaborates the process challenges to transistor scaling that once addressed, enabled meeting Intel's aggressive 10nm technology reliability targets.

1:10 PM

6F.5 **Effects of Far-BEOL Anneal on the WLR and Product Reliability Characterization of FinFET Process Technology**

H. Sagong, H. Kim, S. Choo, S. Yoon, H. Shim, S. Ha, T. Jeong, M. Choe, J. Park, S. Shin, and S. Pae, Samsung Foundry Business, Samsung Electronics,

Far-BEOL forming gas anneal has been used to passivate dangling bonds and to improve integrity of gate dielectric. The reliability study was conducted on 14nm FinFETs to study the effects of anneals using various gases (including high/normal pressure D2, H2, and N2). Despite that high pressure D2 anneal gave best I/O NFET HCI reliability, most of the other anneals also provided reasonable and comparable reliability results that can provide as more cost-effective alternate process approach.

1:35 PM

6F.6 **Bottom-up Methodology for Predictive Simulations of Self-heating in Aggressively Scaled Process Technologies**

D. Singh, O. Restrepo, P. P. Manik, N. Rao Mavilla, S. Pinkett, H. Zhang, E. Cruz Silva, J. B. Johnson, M. Bajaj, S. Furkay, P. Paliwoda, Z. Chbili, C. Christiansen, A. Kerber, S. Narasimha, E. Maciejewski, C.-H. Lin, GLOBALFOUNDRIES

A hierarchical methodology using combination of ab-initio phonon scattering, electron transmission & multi-scale FEM simulations is developed to accurately model material and device level self-heating in FinFET technologies. The framework is applied to capture heat dissipation paths and thermal resistance of FinFETs, interconnects and precision resistors. Excellent agreement against measurements and dependence on process technology is demonstrated across many device types without any fitting. The proposed methodology enables rapid evaluation and process mitigation of self-heating.

2:00 PM

6F.7 **Reliability of Dual-Damascene Local Interconnects Featuring Cobalt on 10nm Logic Technology (Late News)**

F. Griggio, J. Palmer, F. Pan, N. Toledo, A. Schmitz, I. Tsameret, R. Kasim, G. Leatherman, J. Hicks, A. Madhavan, J. Shin, J. Steigerwald, A. Yeoh, C. Auth, Intel

This paper discusses the reliability of a new metallization scheme for 10nm back end of line (BEOL) local interconnect. Electromigration (EM) and time dependent dielectric breakdown (TDDB) on Co fill

interconnects are investigated. Significant innovation in process manufacturing are delivered to meet the reliability challenges of technology scaling. Electromigration time to failure is observed to be at least four orders of magnitude higher for Co fill interconnects compared to Cu alloy metallurgy. Intrinsic TDDB reliability for Co/low-k ILD meets the expectations and surpasses the capability of Cu/low-k ILD systems with E-field acceleration factor of ~5 cm/MV using E-model fit. Wafer level stress induced voiding reliability on Co shows superior intrinsic properties with respect to Cu.

2:25 PM
6F.8 **Transistor Reliability Characterization and Modeling of the 22FFL FinFET Technology (Late News)**
C.-Y. Su, M. Armstrong, L. Jiang, S. A. Kumar, C. D. Landon, S. Liu, I. Meric, K. W. Park, L. Paulson, K. Phoa, B. Sell, J. Standfest, K. B. Sutaria, J. Wan, D. Young and S. Ramey, Intel Corp.

This paper describes the transistor reliability of Intel's 22FFL FinFET technology, which includes an extensive variety of device offerings to enable high performance and low power design options. Detailed evaluations of BTI, TDDB, self-heating, and HCI are included to demonstrate the impact from the various device's pitch, channel length, and threshold voltage. Process integration details are included to highlight the interaction with reliability. In addition, modeling results are shown to be well matched to silicon.