

IRPS Workshop: Providing Enterprise Level System Reliability in the Sub-10nm Technology ERA

1. Background.

The leading-edge technology nodes required for SOC (System on a Chip) have become increasingly complex, requiring device, wiring, and packaging level innovations to sustain the demand for increased processor efficiency, density and performance. These innovations include finFETs, Nanosheet FET, Vertical FETs, Ultra Low K Dielectrics, 2.5D and 3D chip package integrations. With the rapid pace of these innovations (including higher SOC core & socket content), it has become increasingly more difficult for the technology and product reliability teams to effectively reduce the reliability failure rates that meet the enterprise system reliability requirements. From a system level perspective, there are additional reliability challenges with increase in non-volatile memory technology, higher speed I/O interfaces, and off chip accelerators.

The challenges are clear:

- 1) *Identify any new 'systematic' defects that are a direct or indirect result of the new innovative technology and implement process integration modifications to reduce or eliminate these 'systematic' defects.*
- 2) *Enable sufficient 'random' level reliability defect learning given the image size reduction and increased circuit density.*
- 3) *Maximize System Reliability, Availability, & Serviceability (RAS) product and system design features to address the failure rate mechanisms that have the largest potential impact to system reliability.*
- 4) *Ensure sufficient technology reliability lifetime, including BTI, Hot e-, EM, TDDDB, and SER that supports enterprise level system lifetime requirements.*

The key question is, how do we accelerate our technology and product reliability learning to keep pace with the level of innovation and scaling facing the SOC development and manufacturing teams? In the keynote address at IRPS 2017, four major initiatives to address the above challenges were suggested:

- Evaluate Technology Qualification Data Early & Often w/ Emphasis on Functional Stress
- Ensure Intrinsic System Lifetime → Based on Kinetics + Application
- Mitigate Impact of Variability with Process Controls, Chip Design for Manufacturability, & System Design Techniques.
- Build End to End Capability to Screen / Eliminate Subtle Functional Defects (including excursions that may be the result of unique user experience / software)

This list is only a starting point of high level ideas to achieve the learning required in the 10nm / 7nm technology nodes. We would like to explore these in more detail by asking the following questions:

1. Do you think we are experiencing a higher level of new reliability failure mechanisms in the 14nm / 10nm / 7nm technology nodes?
2. How can we more effectively identify new, systematic reliability defects encountered during the early technology development cycles (L1 & L2)?
3. How can we improve our ability to 'screen' reliability defects without impacting system EOL integrity? Including Wafer Level, Module, and System Screens?
4. How can we effectively 'design-in' better chip and system level RAS to mitigate the increases in reliability failure rate?
5. What is the single biggest challenges facing our reliability teams in sub 10nm generation technology

Moderators:



Mr. Ronald Newhart is currently a Distinguished Engineer with IBM working in the Systems & Technology Group, focusing on product engineering and reliability. His first nineteen years with IBM entailed assignments in semiconductor parametric and functional characterization, memory design, yield modeling, and reliability engineering. For the past seventeen years, he has been the lead technology interface to the IBM POWER and Z Series circuit design teams. Ron's contributions have supported the development and manufacturing of more than nine generations of POWER and Z System microprocessors. Ron frequently consults on complex problems that span design, process, and technology for both IBM internal products and other IBM System supplier components. He has co-authored fourteen US Patents and has received several corporate awards.

Mr. Newhart has a Bachelor of Science degree in Electrical Engineering from Pennsylvania State University and a Master of Science degree in System Management from the University of Southern California.



Cameron McNairy is a system reliability, availability and serviceability (RAS) architect for Intel's high performance computing (HPC) efforts. Previously, he drove processor level fault-tolerant solutions as a processor architect for Intel Xeon and Xeon Phi specializing in RAS. Prior to his work in HPC, Cameron was an architect for the Intel Itanium line of processors supporting efforts in RAS, firmware, performance and design. Cameron has been awarded 10 patents, authored or co-authored 8 papers, and has spoken in many forums on a wide variety of topics relevant to the HPC and mission critical computing challenges. He received a BSEE and a MSEE from Brigham Young University and is a member of the IEEE.