6.F.4 **Reliability Studies of a 10nm High-performance and Low power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG**, Anisur Rahman, Javier Dacuna Santos, Pinakpani Nayak, Gerald S Leatherman and Stephen M Ramey, Intel Corporation

Reliability of a state-of the art 10nm FinFET technology. This paper from Intel (Rahman et al.) presents the new architectural features introduced to maximize the density scaling at 10nm (see Fig. 2) and investigates their effect on device reliability. The paper highlights the performance-reliability co-optimization required to develop a successful technology that considers the complex process reliability interactions observed in these ultra-scaled devices. One example is showns in Figure 9 with illustrates an improvement in the 10nm FinFET TDDB breakdown reliability as compared to 14nm generation arising from this performance-reliability co-optimization.

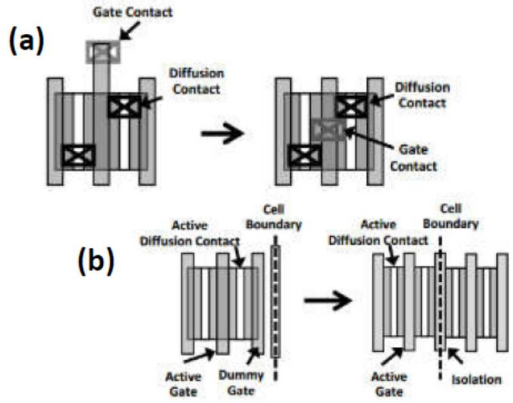

Figure 2 Two new architectural features helped to maximize density scaling at 10nm. (a) Gate contact over active area—eliminating need to extend it over isolation. (b) Minimum isolation at cell boundary, eliminating need for dummy gate.

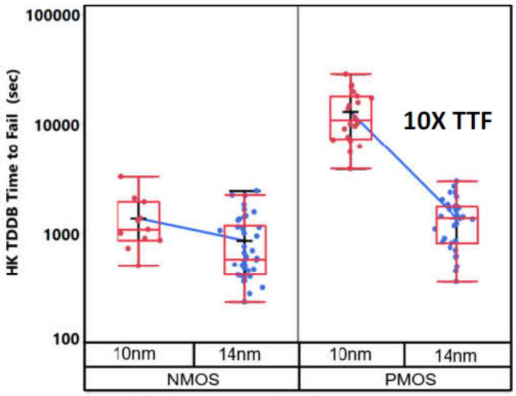

Figure 9 TDDB time-to-fail (TTF) compared between 14nm (4th Gen) and 10nm (5th Gen) HK at matched stress condition and test-structure area. 5th Gen PMOS HK shows substantial intrinsic GOX reliability improvements. NMOS TDDB is matched or better.