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Validating the Robustness of GaN Power Transistors

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Kenichiro Tanaka received the bachelor, the master and the doctor degree of Engineering from the University of Tokyo in 1997, 1999, and 2003, respectively. In his doctoral thesis, he had investigated the optical properties of lead-iodide-based inorganic-organic perovskite materials which have been gaining attention in recent years due to their outstanding properties as a solar cell. After he had investigated as a Special Postdoctoral Researcher in RIKEN institute, Japan, he joined Semiconductor Device Research Center, Matsushita Electronics Corporation (currently Panasonic), Kyoto, Japan in 2007. Since then, he has been engaging in the development of GaN power transistors applicable for high-frequency switching applications. He started his career with the development of crystal growth of GaN on Si substrate, and he has been involving the device design, manufacturing, reliability, and simulation study. He had involved in MHz high-frequency power converter design employing Panasonic's GaN transistors in CPES, Virginia Tech, in the USA from 2015 to 2017. He authored and coauthored 24 technical papers. He is a member of Japanese Journal of Applied Physics and also a sub-committee member of International Reliability Physics Symposium (IRPS) in 2017 and 2018.

In recent years, as GaN power transistors come into widespread use as the promising switches for power converter applications, it is all the more important and inevitable to guarantee their reliability. Firstly, in this tutorial, we will review how we strengthen the robustness of GaN power transistors. We have been incorporating a bunch of technologies to strengthen the robustness of GaN power transistors, which will be briefly discussed. In particular we will introduce a Hybrid-Drain-embedded Gate Injection Transistor, the structure of which is quite effective to ensure the GaN reliability to the commercially-applicable level.

Secondly, we will discuss how we evaluate the robustness of GaN power transistors. The robustness of GaN power transistors should be examined under switching operations as well as under the conventional DC tests standardized for Si power transistors, because severe switching event induces the so-called current collapse, which may end up in the device degradation. The magnitude of current collapse depends strongly on the trajectory of IDS-VDS during the switching event, so is the reliability. Therefore, the concept of Switching Safe Operating Area (SSOA) is proposed recently to define the IDS-VDS limit inside which the device can be switched with safety. In this tutorial, we exemplify the SSOA for our Hybrid-Drain-embedded Gate Injection Transistors (HD-GIT) under the switching for a short period of time. Furthermore, we extract the SSOA for HD-GIT under the switching for much longer period of time, based on the lifetime investigation under accelerated switching condition. We hope that the methodology presented here is utilized to guarantee the robustness of GaN power transistors and it further accelerate the more widespread use of GaN power transistors.