TM2.3
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HBM Design, Test & Reliability Challenges for AI Applications

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Daeyong Shim, VP of SKHynix, received his B.S. degree in Electronic Materials Engineering from KAIST (Korea Advanced Institute of Science and Technology) in 1993, the M.S. degree in Inorganic Materials Engineering from Seoul National University, Seoul, Korea in 1995, and the Ph.D. degree in Electrical Engineering from Seoul National University, Seoul, Korea in 2013. He joined Hyundai Electronics Co. Ltd. (now SK Hynix Semiconductor), Icheon, Korea, as a Research Engineer where he has been working more than 20 years experiences as a DRAM design, test and device engineer worked on processes from 0.32 um to 1y nm. From2016 he is now in charge of HBM product development. His research interests include design of high-bandwidth low-power memory and system applications. He was also a panel speaker in ASSCC 2017.

This tutorial covers recent technology trends of High Bandwidth Memory (HBM)design, test & reliability issues. Current HBM has been developed by dynamic random access memory (DRAM) technology that uses through-silicon vias (TSVs) to interconnect stacked DRAM Core(Cell) die and base die(Logic). After the first successful launching of HBM1 based AMD's Fiji processor which comprises a graphics processor unit (GPU) and four HBM cubes using 2.5D fine-pitch silicon interposer technology, HBM is being used widespreadly in high-performance computing (HPC), data center and network applications.

This presentation introduces the challenges for system integrators to adopt HBM as a high-bandwidth low-power memory solution with small form-factor. Main topics include the reliability issues in HBM 2.5D solution related with TSVs, micro-bumps, fine-pitch silicon interposer and post package DRAM cell repair scheme between HBM and SOC. The thermal &power distribution network (PDN) related HBM design issues and key approaches will be also discussed. Finally, the next generation HBM3 solution will be also briefly introduced.