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An Overview of Chip to Package Interaction and its Impact on Reliability

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Scott Pozder is a Member of Technical Staff at GLOBALFOUNDRIES. He received a B.S. in Physics from Montana State University and a M.S. in Material Science from Colorado School of Mines. Prior to joining GLOBALFOUNDRIES he was at Motorola which then became Freescale working on CPI, 3D wafer and die stacking in addition to MEMS process integration. After Freescale to development projects he participated in development projects for memristors and wafer bonded sensors for life sciences applications. At GLOBALFOUNDRIES his focus area is the CPI reliability of advanced node semiconductor technologies. He is an author or coauthor on over 14 publications in the areas of 3D IC, Advanced Packaging and Cu BEOL and is an inventor on 19 U.S. Patents.

In the early 2000's CPI became a major reliability topic because of the susceptibility for low-k and ultra-low-k dielectric BEOL materials to fail during chip attach to package. With over a decade of interconnect and package material improvements CPI remains a reliability challenge. This is due to factors beyond the continued use of low k films as interconnect dielectric material. These factors include: the increase in device density through scaling and from 2.5/3D integration, decreasing bump size or moving to Cu pillars to enable higher IO counts, increasing package to chip area ratios to accommodate the higher IO counts, the introduction of thinner coreless packages, thinner chips and the evolution package materials. These and other aspects of CPI and their impact on reliability will be covered in this tutorial.