TS2.4
Amit Marathe, Google
Amit Kale, Google

https://www.linkedin.com/in/amit-marathe-1323a9/
https://www.linkedin.com/in/amit-kale-ph-d-93895b2/

Amit Marathe earned his M.S. and Ph.D. in Materials Science and Engineering from the University of California, Berkeley in May 1991 and August 1996 respectively. Amit joined AMD in Sunnyvale CA soon after graduation and then GlobalFoundries in 2009. At AMD and GF, he was leading and managing the Technology & Reliability Development Organization. In 2011, Amit joined Microsoft and was managing the Silicon/Packaging Operations & Reliability Org for all of Microsoft Hardware. Amit joined Google in 2016 where he is heading the SOC/Module Technology and Reliability Engineering & supporting all programs within Consumer Hardware Org at Google.

Amit has co-authored over 40 technical research publications as well as a chapter in a book on Moore's Law Scaling Reliability Challenges. He has chaired sessions at IRPS Conf. and presented "Year in Review" on System Reliability. He has also given keynotes at other International Conferences. He is a co-inventor of over 15 patents granted and over 50 pending US patents in the area of technology & reliability development.

Amit Kale earned his M.S. and Ph.D. in Mechanical engineering from University of Florida, Gainesville in 2005. After completing his Ph.D., Amit joined General Electric Global Research Center in Niskayuna, NY and worked on research and development of jet engines and land based turbines. Amit joined Baker Hughes in 2012 and worked in oil and gas industry for development of predictive analytics and data science for drilling equipments reliability and efficiency. Amit is currently working as a Reliability Program Leader at Google on Moonshot products. Much of Amit's research and industry experience concerns machine learning, data science, reliability analysis and modeling, fracture and fatigue mechanics, and structural design optimization, among other topics. Amit has published over 25 publications in peer reviewed journals and conferences. He is an inventor in two patents and co-inventor in two pending US patents in area of data science and engineering.

Accurate estimation of system level reliability requires a thorough understanding of the failure modes of the various components and modules that make up the system and their interactions with each other. A clear definition of Mission profile is necessary to project the test data to use conditions. With the increasing use of smart devices, mobile technologies and ubiquitous computing, the usage scenarios are getting increasingly complex. As a result, JEDEC based standard Qualification methodologies for components cannot be relied upon to ensure reliability at system level during field usage. This tutorial will introduce the methodology of "Reliability Budgeting" and show how this can be applied at chip level and then at the system level using a tops-down and bottoms-up approach to realize an optimum trade-off between performance and reliability. We will outline the methodology for a rigorous DFMEA process (Design Failure Mode Effects Analysis) which is vital to implement a "Design for Reliability" (DFR approach). The tutorial will also discuss scenarios where system reliability may be improved and demonstration test duration may be reduced by adding redundancy. Using specific test cases, we will also demonstrate the process of optimizing tradeoff between cost of redundancy vs reducing maintenance cost of the system. Finally, a methodology to calibrate component level failure models and test plans is demonstrated from life data on fielded product.