TS2.2
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Introduction to ESD and Latchup Design and Test Methods

Nathan Jack received a Ph.D. in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, in 2012. Since 2012 he has been with Intel Corp. in Oregon as an ESD/Latchup Reliability Engineer. Dr. Jack was the recipient of the Best Poster Award from IRPS, the Best Student Paper Award from the EOS/ESD Symposium and is a two-time recipient of the Outstanding Paper Award from the EOS/ESD Symposium. He has served for the past five years on the technical program and steering committees for the ESD Symposium, International ESD Workshop, and IRPS. He is also an active member of the ESDA/JEDEC CDM Joint Working Group.

The challenges (and opportunities!) facing the ESD and latchup engineer have never been greater. While technology scaling and increasing data rates shrink the ESD and latchup design space, many of the real-world causes of ESD and latchup do not scale. This tutorial is designed as an introduction for those new to or unfamiliar with ESD and latchup. An overview of the real-world events that can cause ESD and latchup damage to ICs as well as the standardized test methods for approximating these stresses (CDM, HBM, system-level ESD, and latchup testing) will be given. On-chip protection and design practices will be reviewed, and examples of failure mechanisms will be given. The tutorial will also touch briefly on the need for improved ESD test standards and factory control to meet the demands of future technology.