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3D Flash Memories: Overview of Cell Structures, Operations and Reliability

Makoto Fujiwara received the B.S. degree in electrical engineering from North Carolina State University, Raleigh, NC in 1992 and the M.S. degree in electrical engineering from Stanford University, Stanford, CA in 1994. He was a research and teaching assistant at Stanford University in 1995. He joined Toshiba Corporation in 1996 where he was responsible for device design and process integration of both bulk and SOI MOSFETs, device/process modeling for TCAD and development of advanced gate stack. From 2005 to 2006, he was a visiting researcher at Stanford University where he worked on physics and modeling of high mobility channel devices. From 2008 to 2011, he was with IBM-Toshiba System LSI Development Alliance in Albany, NY where he conducted development and evaluation of low power CMOS technologies. Currently, he is leading cell device design and characterization for 3D flash memories.

A growth of the memory storage capacity without increasing the area occupation is constantly demanded by the market. The transition from two-dimensional (2D) to three-dimensional (3D) architectures has been the most viable solution to overcome performance and reliability issues from capacity limitations.

In this tutorial, the main reliability mechanisms affecting 3D flash memories will be addressed, providing a comprehensive overview of 3D charge-trap cells and the underlying physics of operation and reliability. Starting from an analysis of basic cell structures and operations, physical mechanisms impacting the reliability of 3D flash memories are reported.