# Storage and Memory – SSD, SD, DIMM: Resiliency in design, system-level considerations and role of usage analytics

**Background:**

Modern leading-edge storage and memory technologies and products are often integrated systems comprising innovations drawn across leading-edge non-volatile and volatile memory, controller, DRAM and even firmware designs. In many cases, innovations of different measure and across various domains need cohesive integration for deriving practical benefits in a reliable manner. Towards that end, inherently designed resilience often becomes a critical enabler for robust storage and memory devices. Critical balance in stress-strength interaction, achieved with appropriately conservative trade-offs in design, are often necessary for appropriately accommodating usage models. In this workshop, one of the intents is to discuss the appropriate levels of resiliency in storage and memory design, towards enabling their robust operational physics.

Can data analytics aid in this endeavor? Wide variances in continuously evolving usage scenarios cover many different stress exposures. Analytics coupled with domain knowledge of system-physics can provide opportunities for understanding usage scenarios of interest, while leveraging machine-learning for system-level models relevant to stress-strength interaction relevant to reliability. Data availability on system-level operational physics can therefore become a key enabler in this quest.

## Moderators

**Jay Sarkar** is a Technologist at Western Digital Corporation (HGST) focused on solid-state storage (SSD) analytics and robustness research and development at the system level. His professional experience of 10 years has included core physics and reliability research and development leading to the first Phase Change Memory technology implementation at Intel and Numonyx (Intel spin-off, now Micron) at 90 nm and 45 nm lithography nodes; and a novel reflective, power-efficient display technology development based on microelectromechanical systems (MEMS) at Qualcomm. He has authored/co-authored 16 peer-reviewed international conference and journal papers across diverse domains of system and device physics, analytics, reliability and process modeling of SSDs, Phase Change Memory, 3-D NAND Flash memory and lower-dimensional electron transport. He has issued or filed/pending patents on machine-learned solid-state storage analytics, Phase Change memory array programming for robustness and MEMS encapsulation design. He earned a PhD in Electrical and Computer Engineering from the University of Texas at Austin (awarded the Ben Streetman Prize for dissertation research), M.S. in Applied Physics from Rice University, Houston and B.S. in Physics from the Indian Institute of Technology, Kharagpur. He is a member of the IEEE and has served on the Technical Program Committee of the International Reliability Physics Symposium.

**Haitham Hamed** has more than 20 Years of experience working on various memory technologies (SRAM, DRAM and Flash) and their end systems. Recently concentrating on SSD system reliability and very low failure rate systems. Worked for a number of startups and large IDMS such as ST Micro, LSI and Avago technologies. Currently working for SK Hynix in their memory Solutions division in San Jose concentrating on SSD Controller Quality & Reliability and aiming to achieve ultra-low failure rate SSD controller. This should easily translate to high reliability SSD Drives for both client and enterprise applications.