

# Emerging memory reliability challenges and opportunities in MRAM, RRAM, PCM, 3DXP

## **Background**

Several non-charge-based nonvolatile memories are categorized as “emerging” memories, not suffering from charge-specific issues like scaling limited by statistical fluctuations from small numbers of stored charges or charge leakage. The workshop will consider each emerging memory technology, including MRAM, PCM, RRAM, and 3D X-point, to discuss their reliability physics and reliability issues. These emerging memories typically employ a two-terminal resistive device combined with a selector, thus the adoption of selection devices will be considered in the form of 1T-1C, 1T-1R, or 1D-1R, the diode selector being the key to practical 3D cross-point memory. However, the discussion will be by no means limited to this topic and other subjects will also be covered such as memory device characteristics, characterization techniques, impacts of variability, and materials choice.

Questions:

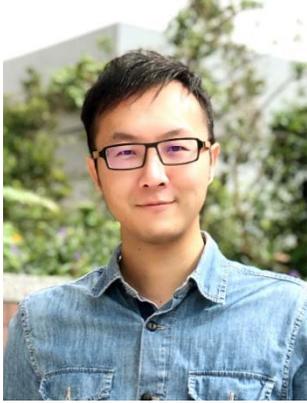
1. What are the top two reliability concerns for each of the emerging memories?
2. Do devices that employ atomic (or ionic) motion to change states have inherent reliability limitations due to the reversibility of the resistance change process? If so, are there failure acceleration methods and models to experimentally predict the limits?
3. Is there a clear separation of intrinsic and extrinsic failures in each of these device types?
4. Is a tradeoff between endurance and data retention time inherent to all of these devices? Same question for endurance – speed and endurance – write energy.

## **Moderators:**



Jon Slaughter is a Principal Research Staff Member and Cognitive Nonvolatile Memory Technologist at IBM Research in Albany New York. Dr. Slaughter has over 20 years of experience in MRAM and related technologies with emphasis on developing new materials and devices for reliable products, including the world's first commercial MRAM products. He worked previously at Motorola, Freescale Semiconductor and Everspin Technologies, Inc. He received his bachelor's degree in physics and mathematics from the University of Wisconsin, River Falls, and doctorate in physics from Michigan State

University.



Dr. Chung-Wei(Jerry) Hsu is a Principal Engineer at TSMC. He received Ph.D in Electronics Engineering, National Chiao Tung University (NCTU), Taiwan, in 2016. He was a visiting scholar in Electrical Engineering and Stanford SystemX Alliance, Stanford University. His research interests include the development of terabit nonvolatile RRAM, reliability Physics and memory device characterization. He joined TSMC in 2016 with Path-Finding team for N5/N3 technology FEOL transistor integration development as well as FEOL module development.