Circuit Reliability
Advanced nodes concerns and CAD tool flows

Moderators:

Matthew Hogan, Mentor, A Siemens Business
Wonjae Kang, Intel
Hiu Yung Wong, Synopsys

Device physics, detailed simulations and angst over the next generation of interconnect electromigration and other reliability rules drive much of the challenges many of us face on a daily basis. In isolated environments, testchips and accelerated testing form the basis for the recommendations that are made to drive reliability design rules. But what about the circuit designs, the layout engineers and our verification and CAD teams? How does the larger ecosystem supporting and executing robust IC design flows benefit from these findings and what form will they take so that next generation designs can be created while keeping up with the aggressive turn-around-times required for market introduction?

Please joins us in this workshop as we discuss best practices and concerns of advanced process nodes and their associated CAD flows. We will start with the challenges facing simulation and how reliability verification and advanced CAD flows, along with foundry supported rule decks can help establish a solid baseline to build upon, including:

- Pre-silicon characterization efforts for reliability, design for reliability(including correct-by-design), and the impact on design rules and reliability verification.
- The wide range of challenges with simulation infrastructures, custom circuits, and modeling of reliability effects including circuit interaction.
- Balancing productivity efficiency with circuit complexity and increasing transistor count with the desire to incorporate 2nd order issues.
- The role of DFT to identify and isolate damage in manufacturing failures and field returns, before the descriptive process of analysis begins.
- Understanding best practices being used by different groups within the industry and the trade-offs on what to simulate, and when.

Share your experience and learn from others as we discuss the challenges we face as we transition to not only the “next” node, but also consider the implications of continuing to use or migrating bulk substrate designs, FD-SOI, finFETs or planar transistors and the legacy IP that has been proven. What are the applications that are driving these decisions and the design choices that are creating an environment for change?

Matthew Hogan, Mentor, A Siemens Business
matthew_hogan@mentor.com
https://www.linkedin.com/in/matthew-hogan-4988263/

Matthew Hogan is a Product Marketing Manager for Calibre Design Solutions at Mentor, a Siemens Business, with over 18 years of design, field and product development experience. He is actively working with customers who have an interest in Calibre® PERC™ or reliability verification. Matthew is an active member of the International Integrated Reliability Workshop (IIRW), is on the Board of Directors for the ESD Association (ESDA), contributes to multiple working groups for the ESDA and is a past general chair of the International Electrostatic Discharge Workshop (IEW). Matthew is also a Senior Member of IEEE, and a member of ACM. He holds a B. Eng. from the Royal Melbourne Institute of Technology, and an MBA from Marylhurst University. Matthew can be reached at matthew_hogan@mentor.com

Wonjae L Kang, Intel
wonjae.l.kang@intel.com

Wonjae L. Kang leads design reliability capability and methodology development efforts at Intel Corporation. Meeting technical challenges with complexity increase reliability mechanism in high-performance and complex designs in IP and SOC designs has been the passion for Wonjae over two decades. Wonjae has technical and engineering management experiences in process, design/CAD enablement and product qualification/ramp. His focus area of expertise is enabling design CAD/Methodology solutions ranging from correct-by-construction to verification for critical reliability mechanisms and design quality interaction issues. Previously he also led an industry-wide initiatives in enabling CAD and design methodology efforts to tackle complexity increase with design automation efforts for Designing-In-Reliability. He received MS and BS in Electrical Engineering from Arizona State University.

Hiu Yung Wong
hiuyung.wong@ieee.org
https://www.linkedin.com/in/hiu-yung-hugh-wong-4274065/

Hiu Yung Wong received his Ph.D. degree in electrical engineering and computer science from the University of California, Berkeley in 2006. Between 2006 and 2009, he worked as a Technology Integration Engineer on 45/32nm NOR flash memory in Spansion Inc., Sunnyvale. Since 2009, he has been with Synopsys Inc., Mountain View, where he is currently a Senior Staff AE in TCAD simulation. His research interests include NBTI and hot carrier degradation simulation in FinFET/nanowire/nanosheet, wide band gap materials (such as GaN, Ga_2O_3 and Diamond) device and reliability/defect simulations, novel semiconductor device design and Design Technology Co-Optimization (DTCO). Part of the activities are reflected in the near 50 publications and patents applied. He is a senior member of IEEE.