Circuit Reliability: In-field healing and repair – serious need or science fiction?

With continued Moore's Law scaling to 7nm node and beyond, CMOS technologies face variability and reliability challenges that impact performance, power, and yield. While static variations can be handled by more robust post-silicon test and binning procedures, dynamic variations are impacted by environmental conditions, activity, and workload. These variations coupled with ever-increasing chip complexity present large challenges for guaranteeing reliability at an acceptable cost. These challenges are becoming especially critical in markets such as automotive and avionics with stringent reliability requirements. While in-field dynamic adaptation to temperature and voltage fluctuations has become standard for many semiconductor devices, techniques for detecting and compensating reliability degradation are still in their infancy [1-3]. Thus the question arises: is in-field healing and repair a serious technology need, or science fiction?

At the device level, various solutions have been examined for reducing impact of wearout issues such as hot-carrier degradation and bias temperature instability: annealing defects at very high temperature in silicon bulk MOSFETS [4,5], using short self-healing in flash memory [6] and in gate-all-around MOSFETs [7], by oxide charge neutralization with opposite-carrier injection [8], and by using forward current in the drain-bulk junction [9]. While promising at the device level, most of these solutions are not feasible to implement in operating circuits. This can be overcome using real-time carrier injections (however the gain in device lifetime is limited [8]) or through the use of forward body bias in FDSOI technology [10], but a high-level methodology is needed from circuit to system level, that is based on a hierarchical framework [3] for the trade-off between performance, activity, and power consumption.

At the circuit level, techniques have been demonstrated for detecting and responding to dynamic fluctuations in temperature, voltage, and workload demand. It is now feasible to extend these techniques to monitor and maintain reliability in the field. For example, an in-situ mission profile recorder [11] used with thermal sensors can dynamically adapt the frequency or supply voltage in response to changes in activity, variability, or aging that are detected by in-situ slack monitors [3,12,13]. These adaptive techniques will become more important as reliability requirements become more stringent, and as process scaling becomes more difficult. However, advancements are required not just on the detection circuits and adaptation techniques, but also on dedicated analog and digital design flows to enable reliability-aware design platforms and a full self-adaptive design methodology from devices to software [14].

Improving in-field reliability further will require advancements in the entire design hierarchy from devices to software. Early-life failures due to latent defects or electromigration cannot easily be detected with monitor circuits, and adaptive voltage and frequency techniques cannot repair permanent failures. Instead, techniques for core/circuit self-test and repair [15-16] are needed, as well as methods to maintain system performance as self-test is performed, and the necessary level of redundancy to repair failures in a way that is invisible to the application (and the customer). These techniques have been explored for high-reliability server processors but are difficult and expensive to adopt. Is this level of reliability monitoring and repair necessary in other applications? At what point does the reliability benefit of these techniques justify the investment in cost and complexity? How can the dramatic increase in device count that comes with every process generation be used to not only add features and improve performance, but also improve reliability and yield? When will our semiconductor devices "heal themselves“?

References

[1] J.W. Tschanz, K.A. Bowman, S. Walstra, M. Agostinelli, T. Karnik, V. De, "Tunable replica circuits and adaptive voltage-frequency techniques for dynamic voltage, temperature, and aging variation tolerance", Symposium on VLSI Circuits, 2009.

[2] K. A. Bowman, J. W. Tschanz; S.-L. L. Lu; P. A. Aseron; M.M. Khellah; A. Raychowdhury; B.M. Geuskens; C. Tokunaga; C. B. Wilkerson; T. Karnik, V. K. De, "A 45nm Resilient Microprocessor Core for Dynamic Variation Tolerance," *IEEE J. Solid-State Circuits*, pp. 194-208, 2011.

[3] V. Huard, S. Mhira, F. Cacho, A. Bravaix, "Enabling robust automotive electronic components in advanced CMOS nodes", Microelectronics Reliability, Vol. 76-77, pp. 13-24, 2017.

[4] J.C. King, C. Hu, Effect of Low and High Temperature anneal on process-induced damage of gate-oxide, EDL, Vol. 15, N° 11, p.475, 1994.

[5] C. Benard, J.L. Ogier, D. Goguenheim, "Total Recovery of Defects Generated by Negative Temperature Instability (NBTI)", in Int. Integrated Reliab. Workshop (IIRW), p. 7, 2008.

[6] H-T. Lue, P-Y. Du, C.-P. Chen, W.-C. Chen, C.-C. Hsieh, Y-H. Hsiao, Y-H. Shih, C-Y. Lu, "Radically Extending the Cycling Endurance of Flash Memory (to > 100M Cycles) by Using Built-in Thermal Annealing to Self-heal the Stress-induced Damage", in Proc. of IEDM, p. 199, 2012.

[7] J-Y. Park, D.-Il Moon, M-L. Seol, C-K. Kim, C-H. Jeon, H. Bae, T. Bang, Y-K. Choi, "Self-Curable Gate-All-Around MOSFETs Using Electrical Annealing to Repair Degradation Induced From Hot-Carrier Injection", IEEE Trans. on Electron Dev., Vol. 63, N°3, pp. 910-915, 2016.

[8] A. Bravaix, , F. Cacho, X. Federspiel, C. Ndiaye, S. Mhira, V. Huard, "Potentiality of Healing Techniques in Hot-Carrier Damaged 28nm FDSOI CMOS nodes", Microelectronics Reliability, Vol. 64, pp.163-167, 2016.

[9] G-B. Lee, C-K. Kim, J-Y. Park, T. Bang, H. Bae, S-Y. Kim, S-W. Ryu, Y-K. Choi, "A Novel Technique for Curing Hot-Carrier-Induced Damage by Utilizing the Forward Current of the PN-Junction in a MOSFET", IEEE Electron Dev. Lett., Vol. 38, N°8, pp. 1012-1014, 2017.

[10] C. Ndiaye, V. Huard, X. Federspiel, F. Cacho, A. Bravaix, "Performance vs. Reliability Adaptive Body Bias Scheme in 28nm & 14nm UTBB FDSOI nodes", Microelectronics Reliability, Vol.64, pp. 158-162, 2016.

[11] M. Saliva, F. Cacho, V. Huard, X. Federspiel, D. Angot, A. Benhassain, A. Bravaix, L. Anghel, "Digital circuits reliability with in-situ monitors in 28nm fully depleted SOI", Best Paper of Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 441 – 446, 2015.

[12] S. Mhira, V. Huard, A. Bravaix, A. Benhassain, F. Cacho, S. Naudet, A.Jain, C. Parthasarathy, "Cognitive approach to support dynamic aging compensation", Best Paper of International Tests Conference, Bangalore (Inde), pp. 1-7, 2017.

[13] S. Mhira, V. Huard, F. Cacho, A. Benhassain, A. Jain C. Parthasarathy, S. Naudet, A. Bravaix, "Dynamic Adaptive Voltage Scaling in Automotive environment", Outstanding Paper of IEEE International Reliability Physics Symposium (IRPS), 3A-4.1 3A-4.7, 2017.

[14] RESIST Project - CT217, Labellized and funded by the French pôles (DGE) and European fundings CATRENE (Eureka Cluster), http://www.catrene.org/web/downloads/profiles_catrene/catrene-project-profile-resist.pdf

[15] Y. Li, S. Makar, S. Mitra, "CASP: Concurrent autonomous chip self-test using stored test patterns", *Proc. IEEE/ACM Design Automat. Test Eur.*, pp. 885-890, Mar. 2008.

[16] Michael D. Powell, Arijit Biswas, Shantanu Gupta, and Shubhendu S. Mukherjee. 2009. Architectural core salvaging in a multi-core processor for hard-error tolerance. In *Proceedings of the 36th annual international symposium on Computer architecture* (ISCA '09). ACM, New York, NY, USA, 93-104.

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