Circuit Reliability: In-field healing and repair – serious need or science fiction?

With continued Moore's Law scaling to 7nm node and beyond, CMOS technologies face variability and reliability challenges that impact performance, power, and yield. While static variations can be handled by more robust post-silicon test and binning procedures, dynamic variations are impacted by environmental conditions, activity, and workload. These variations coupled with ever-increasing chip complexity present large challenges for guaranteeing reliability at an acceptable cost. These challenges are becoming especially critical in markets such as automotive and avionics with stringent reliability requirements. While in-field dynamic adaptation to temperature and voltage fluctuations has become standard for many semiconductor devices, techniques for detecting and compensating reliability degradation are still in their infancy [1-3]. Thus the question arises: is in-field healing and repair a serious technology need, or science fiction?

At the device level, various solutions have been examined for reducing impact of wearout issues such as hot-carrier degradation and bias temperature instability: annealing defects at very high temperature in silicon bulk MOSFETS [4,5], using short self-healing in flash memory [6] and in gate-all-around MOSFETs [7], by oxide charge neutralization with opposite-carrier injection [8], and by using forward current in the drain-bulk junction [9]. While promising at the device level, most of these solutions are not feasible to implement in operating circuits. This can be overcome using real-time carrier injections (however the gain in device lifetime is limited [8]) or through the use of forward body bias in FDSOI technology [10], but a high-level methodology is needed from circuit to system level, that is based on a hierarchical framework [3] for the trade-off between performance, activity, and power consumption.

At the circuit level, techniques have been demonstrated for detecting and responding to dynamic fluctuations in temperature, voltage, and workload demand. It is now feasible to extend these techniques to monitor and maintain reliability in the field. For example, an in-situ mission profile recorder [11] used with thermal sensors can dynamically adapt the frequency or supply voltage in response to changes in activity, variability, or aging that are detected by in-situ slack monitors [3,12,13]. These adaptive techniques will become more important as reliability requirements become more stringent, and as process scaling becomes more difficult. However, advancements are required not just on the detection circuits and adaptation techniques, but also on dedicated analog and digital design flows to enable reliability-aware design platforms and a full self-adaptive design methodology from devices to software [14].

Improving in-field reliability further will require advancements in the entire design hierarchy from devices to software. Early-life failures due to latent defects or electromigration cannot easily be detected with monitor circuits, and adaptive voltage and frequency techniques cannot repair permanent failures. Instead, techniques for core/circuit self-test and repair [15-16] are needed, as well as methods to maintain system performance as self-test is performed, and the necessary level of redundancy to repair failures in a way that is invisible to the application (and the customer). These techniques have been explored for high-reliability server processors but are difficult and expensive to adopt. Is this level of reliability monitoring and repair necessary in other applications? At what point does the reliability benefit of these techniques justify the investment in cost and complexity? How can the dramatic increase in device count that comes with every process generation be used to not only add features and improve performance, but also improve reliability and yield? When will our semiconductor devices "heal themselves"?

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