2018 IRPS Workshop: Challenges and Advances in Advance Node Interconnect Reliability

Background

Several new areas of challenge exist for interconnect reliability stemming from the ever present drive for dimensional scaling and RC delay reduction. The challenge associated with dimensional scaling and variability is a consistent theme for advance nodes and is further exacerbated by minimal to no scaling in operating voltages. New materials for inter-layer dielectrics, dielectric spacers, etch stop layers, Cu/ILD barriers are introducing new challenges for interconnect reliability in the Back-End-of-Line (BEoL) and in the Middle-of-Line (MoL). New integration and patterning schemes like Air Gaps, self-aligned vias and contacts, and EUV patterning might offer a balance of reliability enhancing and detracting aspects. Beyond the direct assessment of intrinsic reliability in interconnects there is an additional set of challenges to assess, predict, and control end product reliability which incorporates other aspects like latent defectivity, package stress, and the challenge of assessing metallization reliability in product like configurations. In this workshop we will focus the discussion on the key areas of interconnect challenge in the present and near term, and discuss the prospects for advancement in reliability methodology that might be used to mitigate these challenges for end product reliability spanning across various market segments.

Workshop Co-Moderators:

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Dr. Patrick Justison received his Ph.D. and M.S.E. in materials science from the University of Texas and his B.S. in materials science from Lehigh University. He has been with GLOBALFOUNDRIES since its inception in 2009, after joining AMD in 2008. He currently the leads the BEoL reliability team in Malta, NY. He and his team are responsible for all aspects of interconnect reliability, including development, qualification, PDK support, and development of novel methodologies for advanced technology nodes. Previously, he was with Freescale in Austin, TX where he also focused on BEoL reliability topics.

Dr. Rahim Kasim (Rahim.kasim@intel.com) is a Reliability Manager in Intel's Logic Technology Development Group working primarily on MOL/BEOL reliability across 14nm/10nm and 7nm Technology nodes. He joined Intel in 2005 after receiving Ph.D. and M.S degrees in Electrical Engineering from Arizona State University. His interests includes BEOL/MOL dielectric Reliability and Interconnect Reliability