Advanced packaging reliability: 2.5D, 3D and fan-out packaging for system scale

Background:

Recently advanced packaging technologies of 2.5D, 3D and fan-out have attracted attention for realizing high performance and multi-functionality systems. But heterogeneous integration of various materials and devices for 2.5D, 3D, fan-out packaging has crucial reliability challenges. Moreover, a trend of 3D/2.5D packaging towards thinner chip, more layer stacking, and more joining density to maximize area efficiency. Fan-out packaging requires more fine width/space, and multi-layers of Cu RDL for multi-dies integration. These trends could induce severe potential reliability challenges. Therefore, advanced packaging reliability becomes a hot research topic for further system scale. The main objective of this workshop is to discuss the reliability challenges and possible solutions for mass volume manufacturing start. However, the discussion will be by no means limited to this topic and other subjects will also be covered such as characterization/simulation techniques, impact of materials choice.

Moderators:

Kang-Wook (Kriss) Lee is currently VP, R&D, Amkor Technology Korea. He received the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 2000. From 2000 to 2001, he was a Researcher with Japan Science and Technology Corporation, Sendai, Japan. From 2001 to 2002, he was a Postdoctoral Researcher with the Department of Electrical, Computer, and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY, USA. From 2002 to 2008, he worked with Packaging Development Team, Memory Division, Samsung Electronics Ltd., Korea, as a Principal Engineer, where he led the research and development of TSV based 3D packaging technologies. From 2008 to 2016, he was a professor with Tohoku University, Sendai, Japan. He has led the development of 3D hetero-integration technology for multi-functional convergence systems, multi-chip self-assembly technology, exa-scale 2.5D/3D integration technology, and the reliability studies of 3D-IC. Especially, he worked pioneerly the studies about the impacts of 3D integration process such as Cu TSV formation, wafer thinning and micro-joining of thin chip on reliability of 3D stacked devices by leading the world.

He is a Senior Member of the IEEE.

Emre Armagan joined Intel Corporate Quality Network (CQN) organization as Assembly Test Technology Development Quality and Reliability (ATTD Q&R) engineer in 2011. He is currently ATTD Q&R Senior Engineering Manager responsible for assembly and substrate process technology development. He has worked on silicon far backend, FLI and package quality and reliability; and supported pathfinding and technology development for various multi-die products and 2.5D/3D package integration, including Intel's Embedded Multi-Die Interconnect Bridge (EMIB) solution. He has authored/co-authored multiple papers as invited, journal and conference publications and has

awarded and pending US patents. His industry engagements include contributions to IRPS and InterPACK technical committees and journal reviews.