5.C.2 **All-Digital PLL Frequency and Phase Noise Degradation Measurements Using Simple On-Chip Monitoring Circuits** by Gyusung Park, Bongjin Kim, Minsu Kim, *Vijay Reddy and Chris H. Kim , University of Minnesota, *Texas Instruments

The purpose of this work is to understand the impact of device aging on frequency and phase noise degradation of an All-Digital Phase Locked Loop (ADPLL) circuit. An on chip phase noise and Digitally Controlled Oscillator (DCO) monitor provides a fast and accurate in situ measurement and communication to the external world through a cheap and simple serial interface. This eliminates the need of expensive and complex external test setup like high frequency sampling scope or a spectrum analyzer, that would be prohibitive for some low cost test applications or environmental conditions (eg. Space applications)

Despite the fact that the on-chip monitor is based on standard digital circuits such as counters, flip-flops, and a variable delay line, it achieves a frequency degradation measurement accuracy of 0.01% within a few microseconds.

Such measurements provide the magnitude of required up-front design margin for proper end of life operation without over-designing. They also show that the natural recovery mechanism is not adequate to resolve this degradation issue and additional anneal will be needed for full recovery.

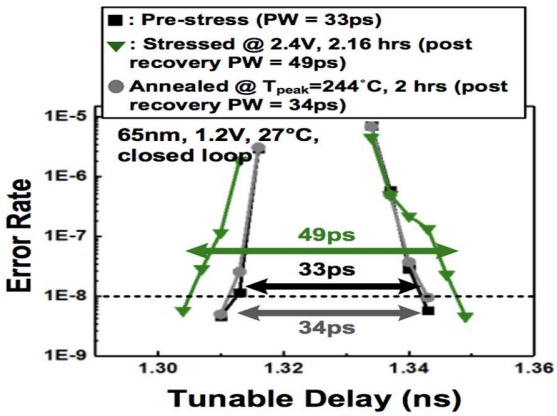

Fig. 11. Measured closed-loop phase window curves for pre-stress, stressed, and annealed DCOs.