4C.1 **Scaling Trends and Bias Dependence of the Soft Error Rate of 16 nm and 7 nm FinFET SRAMs** by Balaji Narasimham, Saket Gupta, Dan Reed, J. K. Wang, Nick Hendrickson, Hasan Taufique, Broadcom

This work presents the scaling trends in the alpha and neutron SRAM SER from planar to two FinFET process nodes. While the first process scaling from planar to FinFET resulted in large SER reduction, the subsequent scaling from 16 nm to 7 nm FinFET is shown to follow the bit-cell area reduction. Extensive data collected across a range of supply voltages in planar and FinFET processes show strong exponential bias dependence of SRAM SER for FinFET processes, while for the planar process it follows a linear trend. The results presented in the paper highlight the importance of understanding the SER scaling trends and bias dependence for FinFET-based circuits as well as developing mitigation schemes based on the intended application and operating voltage range.