3D Transistor Reliability: Hot Carrier (HC) Degradation

Background

In recent technology nodes, Hot Carrier-induced degradation is coming up arguably as the most concerning FEOL degradation mechanism. As a consequence of its inherent physical complexity, HC degradation requires careful experimental characterization and thorough modeling for relevant reliability projections. In this workshop, we will discuss recent trends in HC literature, focusing on a list of topics related to current characterization practice, modeling approaches, and device engineering for HC mitigation, with the goal of assessing the existence of a consensus view of the reliability community on each of these aspects.

Discussion topics:

- HCD is traditionally studied at worst-case bias (i.e., maximum impact ionization) or at V_G=V_D: is this still enough? Does the community see a need to move toward more comprehensive studies in the whole {V_G,V_D} bias space? Is it acceptable to simply rescale the degradation measured in DC at worst-case bias to the actual AC workload?
- Does the bias history affect the device degradation (e.g., is BTI the same on a device which already suffered severe HC degradation)?
- How can one de-embed the SHE impact on the degradation consistently across the whole {V_G,V_D} bias space?
- Is variability of the HC degradation relevant? If yes, what experimental approaches are effective to characterize it across the {V_G,V_D} stress bias space?
- Is Off-state hot carrier stress also a relevant degradation mode for Si finFETs? If yes, which unified failure criterion can we use for any stress {V_G,V_D} combination? (note: the typical shifts of I_{Dsat} and V_{th} are not enough for Off-state degradation as other device metrics as I_{off}, SS, GIDL, also degrade)
- HC mitigation at the device level: which device design strategies are effective without penalty on the device performance (typical trade-offs: abrupt junctions --> better short channel controls --> higher electric field peak --> worse HC!; high-mobility channels (SiGe) --> larger carrier mean free path --> worse HC!)
- Theoretical studies focus on individual physical degradation modes (e.g., Single-Vibrational Excitation vs. Multi-Vibrational Excitation for the Si-H bond breaking): how should one decouple these modes and what acceleration model should one adopt to project the degradation of devices during real use (i.e., bias spanning dynamically a given trajectory in the {Vg,Vd} space)?
- Are empirical models (based on physical understanding) sufficient for HC degradation or should we adopt complex full physics models (including, e.g., carrier distribution functions; electron-electron scattering impact on the energy tails, etc.)?
- What classes of circuitry is HCI a concern for (clock distribution, high-speed IO, SerDes, etc.) vs. not (data paths, sequentials, SRAM, etc.)?

Moderators

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