3D Transistor reliability: BTI

Background BTI - Measurements, Modeling and Variability

1) Measurements - the one point drop down method is kind of widely used to sense Vt shift. However, what should be the measurement speed, stress bias range and stress time range (to minimize recovery and EOL extrapolation errors) for bench test? Is there any concern regarding corrections required for long measurement delay typically encountered for HTOL tests? Also, is Vt sense enough, or do we need to sense other parameters (like Idlin etc) as well?

2) Modeling - Modern transistors are 3D (with quantum effects in the channel), and actual operation involves mixing of HCI, BTI and self heating effects. Is there a need to invoke TCAD for accurate device level simulation (and isolation of different effects)? On the SPICE compact model side - is DC enough, or there is need for good AC (eg duty cycle) modeling? Are the existing CAD vendor frameworks good enough (is there any consistency between different foundry models), or there is need to develop an uniform, consistent compact model platform? Is there any benefit to include ageing/BTI in DTCO efforts? Finally, with new materials (SiGe channel, III-V channel, N, F, dipole, trace elements in the gate stack), is there a requirement to bring in ab-initio models for prediction?

3) Variability - What are the relative importance of time-zero (eg process related) and BTI variability? Are these fully uncorrelated or weakly correlated? What is the importance of RTN? Does RTN change after BTI stress?

Moderators

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Chadwin D. Young received his B.S. degree in Electrical Engineering from the Univ. of Texas at Austin in 1996 and his M.S. and Ph.D. in EE from the North Carolina State University in 1998 and 2004, respectively. In 2001, he joined SEMATECH where he completed his dissertation research on high-k gate stacks and continued this research at SEMATECH working up to Senior Member of the Technical Staff on electrical characterization and reliability methodologies for the evaluation of high-k gate stacks on current and future device architectures. He joined (09/12) the Materials Science and Engineering Department at the University of Texas at Dallas as an Assistant Professor where his research focus is on electrical characterization and reliability methodologies for the evaluation of future materials and devices. He has authored or co-authored 250+ journal and conference papers. He has served: on the management or technical program committees of IIRW, IRPS, SISC, IEDM, WoDiM; as Guest Editor for IEEE Transactions on Device and Materials Reliability; and as a peer reviewer for several journals. He is currently a Senior Member of IEEE.