GaN Reliability and standardization – Workshop IRPS 2017

Moderators: Matteo Meneghini and Tim McDonald

Participants: approximately 50

Tim McDonald, INFINEON – GaNSPEC DWG – Introduction and main activities

JESD94B gives guidelines, product requirements, but…what are the main degradation processes? Application-specific qualification strategy is needed. How to develop the reliability models for each degradation process (JEP122, JESD91)?

Three levels:

1. Mission profile
2. GaNSPEC DWG guidelines
3. Outputs: reliability procedures, test methods, datasheet parametrics

Organization of GaNSPEC DWG: there is a steering team, in charge of providing guidelines and templates to focus teams to standardize expectations. Then focus teams are self directed (Reliability standards and qualification, data sheet structure, and test methods).

Major milestones for each focus team: everything started at WIPDA 2016 (review of existing literature, propose focus areas), at APEC 2017 the first list of proposed topics was validated. Goal is to complete a first round of guidelines and best practices before WIPDA2017.

What comes later? The definition of the standards!

The proposed items for guidelines and standards are: reliability (list of failure mechanisms, focus on charge trapping, corresponding acceleration and stress procedures), test (dynamic RDSon, thermal resistance, SOA), datasheet (include the effects of dynamic RDSon, …)

Key takeaways: recognition of standards ability to increase ramp of applications, important to agree on the call for actions, importance of expanding upon existing standards, define path from best practices and guidelines from JEDEC.

Sameh Khalil: Mission profile driven approach for qualification of GaN-based power devices

The problem is to go from application profile to an equivalent stress condition. TDDB is taken as a model. The entries of the model are: list of bias, temperature and time. Then a law to describe the degradation process must be defined. After that, the application profile must be converted into an equivalent stress condition. It all depends on the activation energy.

The main questions are:

› what are the arguments and the counter arguments to generate standard mission-profile(s) that drives future qualification and Reliability testing guidelines/standards?

› what are the arguments and counter arguments for adopting a methodology that outlines the procedure to address the wide range of device designs and wide range of applications, their end use conditions and environmental specifics? [ref: JESD94B*]

› or preference should be to prescribe a minimum set of tests and make recommendations for additional mission-profile driven methodology that addresses wide range of applications and use conditions

Bob Kaplar: charge trapping phenomena

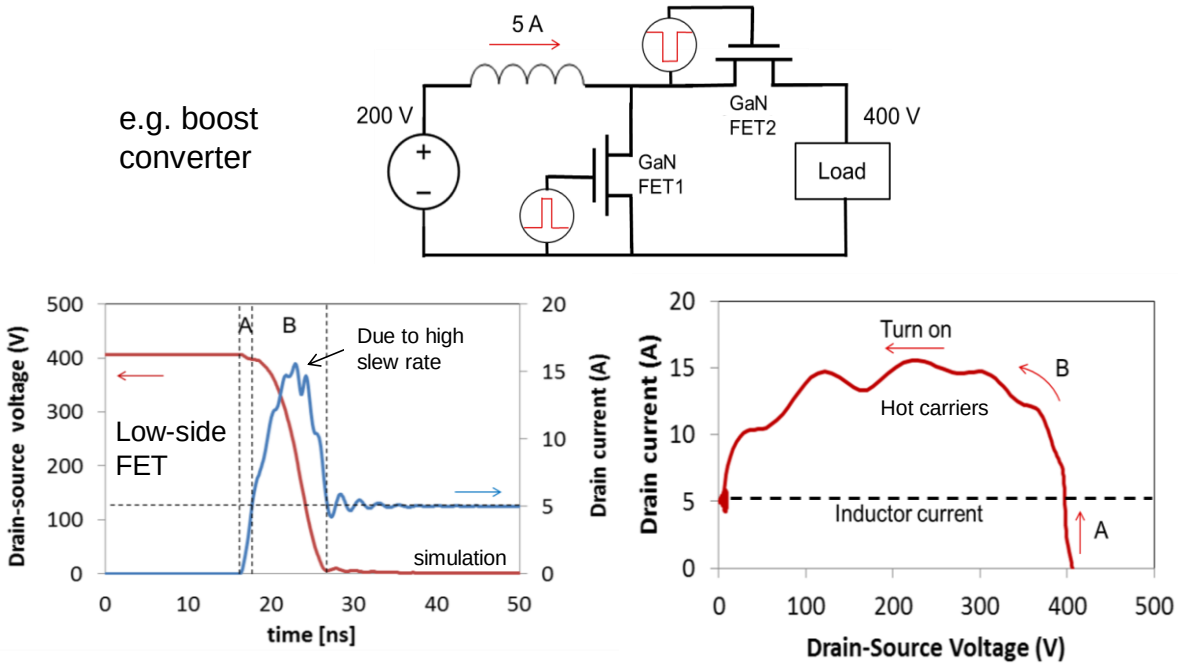
- GaN has many traps! Do all of them play a role?
- Simultaneous trapping process may play an important role, how to study each of them?
- What is the physical location of traps? In the barrier? In the Buffer?
- Some traps are thermally-activated, some other have a temperature-dependent behaviour: can this help to identify the physical origin?

Discussion topics have been:

- How should trap-dependent parameters be handled in terms of reliability guidelines?
- How universal are the observed trapping phenomena? How much do they depend on the specifics of the epi and device design?
- Do we really need to understand the physics of the trapping processes? Or an empirical approach is sufficient?
- Are trapping-related problems being solved?

Sandeep Bahl: Hard switching

During operation, HEMTs are subject to Hard switching, see below:



The FET is subject to repetitive hot-carrier stress, SOA boundaries, and high slew-rates.

Discussion topics have been:

- What failure mechanisms does hard-switching cause?

- How did the Si industry deal with this issue
- Who would be responsible for assuring hard-switching robustness – the foundry/fab or their customer?
- What is switching SOA?
- Does SOA degrade with usage?

Kurth Smith: Converse Piezoelectric effect

Kurt reviewed the most recent papers on the converse piezoelectric effect in GaN transistors, concluding that this is not supposed to be a major issue in GaN-based power devices. He stimulated the discussion on this topic, and summarized the latest results presented in the literature.

Matteo Meneghini: TDDB in power GaN transistors

Matteo covered the topic of time-dependent breakdown in power GaN transistors, by summarizing recent results obtained on Schottky-gate transistors and MIS devices; he also demonstrated that transistors with p-GaN gate may show a time-dependent failure when submitted to stress at positive gate voltage, and stimulated the discussion on these topics.