2023 IEEE International Reliability Physics Symposium (IRPS)

Program

Monterey, California, USA
26 March – 30 March 2023

IRPS
International Reliability Physics Symposium

IEEE

IRPS 2023 General Chair Welcome Message

Welcome to the 61st IRPS conference in-person in Monterey, California, and hosted virtually by Underline! On behalf of the management committee and board of directors, we are extremely pleased to offer a second year of hybrid conference with oral presentations available live virtually during Pacific Time Zone. IRPS is the preeminent conference for timely research on Reliability Physics of devices, materials, circuits, and products used in the electronics industry; this is where important reliability challenges and solutions are first discussed. The live hybrid experience includes morning Keynote Sessions, all technical program oral presentations, and a record setting 28 Tutorials. Videos will be posted within a few days for replay up to one year later. An email to all registrants has been sent out and online help is available during the conference. Once logged in, the simple way to re-enter Underline is through the Ex Ordo mobile app.

We expect this hybrid format to be an excellent way to attend IRPS 2023 and absorb a lot of fabulous content. Virtual attendees will be able to ask authors questions through the Underline platform. Gather.Town also allows virtual attendees the opportunity to meet up with fellow virtual attendees for impromptu conversations through-out the course of the conference. One may enable Gather.Town with one browser screen to signal to others that they are available for conversations with their name. Gather.Town technology has chat, audio, and video capability.

IRPS 2023 kicks off Sunday, March 26th Tutorials beginning 9am PT and continuing through 2:30pm PT on March 27th. IRPS Tutorials are a supreme method for the beginner, the intermediate, and the expert to become familiar with the basic concepts of semiconductor reliability engineering to advanced topics of reliability in new areas such as 2D materials or quantum computing. Tutorials are followed by the ever-popular Reliability Year in Review (YIR) which are three summaries of the last year's publications featuring soft errors, SiC devices, and FEOL reliability of FINFET, nanowires, and nanosheet FETs.

Our 2023 Keynotes are solely comprised of senior executives from four notable companies beginning with the topic of continuing Moore's Law and reliability trends from Intel's Ann Kelleher followed by Transforming industries with trustworthy cloud to edge compute platforms form NVIDIA's Gary Hicok. Wednesday morning commences with AMD's Mark Fuselier covering "Reliability Challenges for the next decade of high performance compute". Thursday morning features Ampere Computing's Rohit Vidwans presenting on "Building Reliability into the Modern Cloud".

The technical program has 3 parallel tracks with 18 technical sessions starting each day at 8am PT and concluding at nearly 6pm PT. The full program can easily be viewed here, at a glance and presentation descriptions can be found here, in the Ex Ordo app, or within Underline. The technical program committee consists of 250 experienced industry, university, and government agency diverse individuals who have all contributed towards IRPS previously or whose expertise IRPS has invited. Truly, the technical program committee is the "backbone" of IRPS and we seek to have a thriving committee with both fresh and seasoned eyes to review submitted abstracts. All of the management committee and board of directors served several years on the TPC. This year's technical program focus topics are

embedded-in-product memory/neuromorphic compute, GAA-nanosheet-RibbonFETTM-Forksheets, and 3D IC advanced packaging.

Workshops and the Poster Reception will be LIVE only and are only available for in-person attendees. They will not be recorded or made available to virtual attendees. Poster presentations have a short video for virtual attendees. We encourage virtual attendees to ask questions or post comments about the papers using Q&A box on the Underline platform. Virtual attendees can start discussion before the conference begins, and continue after it ends.

IRPS and the International ESD workshop have restarted a tradition of being co-located, with IEW registrants having full access to both IRPS and IEW technical program.

At the conclusion of the conference, IRPS will have both in-person and virtual prizes awarded randomly to survey participants. In-person attendees must be present to win. Virtual attendees must include their valid, registered email address to win. The number and level of the prizes will be directly scaled with the number of registrants, so please be sure to fill out the prize surveys in the Ex Ordo app!

Finally, I would like to express my extreme gratitude to our patrons and exhibitors, whose support makes IRPS possible. And to all of you, our in-person and virtual attendees, for supporting this symposium for sixty-one years!

Chris Connor, General Chair

of 2023 IRPS Management Committee

2023 IEEE International Reliability Physics Symposium - *Tutorial & Year-in-Review Program-at-a-Glance*

Sunday • March 26

Time	Regency Main	Regency I-II-III	Regency IV-V-VI	Big Sur
	TUT 1	**TUT 2**	**TUT 3**	**TUT 4**
9:00 AM	Introduction to Reliability Physics and Engineering, *Joe McPherson, McPherson Reliability Consulting LLC*	Machine Learning for Integrated Circuit and Semiconductor Device Reliability Analysis *Elyse Rosenbaum, University of Illinois at Urbana-Champaign*	BEOL and MOL Reliability: *Shinji Yokogawa, The University of Electro-Communications*	LDMOS Reliability: Mechanisms, Methods and Challenges *Guido Sasse, NXP*
10:30 AM	Break - Regency Terrace			
	TUT 5	**TUT 6**	**TUT 7**	**TUT 8**
11:00 AM	FEOL Reliability in Advanced CMOS Nodes *Jen-Hao Lee & Pei Jean Liao, TSMC*	Impedance Spectroscopy of the MOS Systems *Paul Hurley, Tyndall National Institute University College Cork*	Various Reliability Issues in DRAM Cell Transistors *Junsoo Kim, Samsung*	RRAM Based AI and Reliability *J. Joshua Yang, University of Southern California*
12:30 PM	Lunch			
	TUT 9	**TUT 10**	**TUT 11**	**TUT 12**
1:30 PM	BTI in Advanced HKMG for Future CMOS Tech Nodes *Jacopo Franco, imec*	Emerging Memories Reliability: From Device to Applications *Cristian Zambelli, University of Ferrara*	Heterogenous Integration Reliability Challenges and Roadmap *Richard Rao, Marvell Technology*	MEMS Reliability *Ashwin Seshia, Cambridge University*
3:00 PM	Break - Regency Terrace			
	TUT 13	**TUT 14**	**TUT 15**	**TUT 16**
3:30 PM	Reliability Characterization of CMOS Ring Oscillator Circuits in scaled CMOS Technologies *Andreas Kerber, Intel*	Design for Reliability in Product Development *Ranjani Muthiah, Google*	Reliability Challenges for Si Photonics Products *Arif Zaman & Quan Tran, Intel*	Reliability of encapsulating molding compounds for electronic packaging subjected to high field and different environmental conditions *Susanna Regianni, University of Bologna*
5:00 PM	Adjourn			

Monday • March 27

Time	Regency Main	Regency I-II-III	Regency IV-V-VI	Big Sur
	TUT 17	**TUT 18**	**TUT 19**	**TUT 20**
8:30 AM	Device and Interconnect Reliability Implications for Digital and Analog Circuit Design *Sachin Sapatnekar, University of Minnesota*	The Role of Defects in the Dynamic Lifetime of GaN Power Devices *Clemen Ostermaier, Infineon Technologies*	Radiation Effects in a Post-Moore World *Dan Fleetwood, Vanderbilt University*	Reliability and Variability of CMOS Devices at Cryogenic Temperatures *Alexander Grill, imec*
10:00 AM	Break - Regency Terrace			
	TUT 21	**TUT 22**	**TUT 23**	**TUT 24**
10:30 AM	Physical Modeling of Reliability Challenges in SiC Power Devices *Michael Waltl, Institute for Microelectronics, TU Wien*	Automotive Electronics Reliability – Challenges and Opportunities *Pradeep Lall, Auburn University*	Soft Errors – From Simple Devices to Complex Systems *Indranil Chatteejee, Airbus*	Reliability of Semiconductor Spin Qubits for Quantum Computing *Micahel Jura, HRL Laboratories*
12:00 PM	Lunch			
	TUT 25	**TUT 26**	**TUT 27**	**TUT 28**
1:00 PM	Insulators for Devices Based on 2D Materials *Tibor Grasser, TU Vienna*	Ferroelectric Hafnium Oxide Based FeFETs - Device Reliability for Non-volatile Memories and Beyond *Stefan Slesazeck, NamLab*	RF Si CMOS and GaN Reliability for 5G/mmWave/RF Applications *Purushothaman Srinivasan, GlobalFoundries & Don Gajewski, Wolfspeed*	Contactless Fault Isolation (CFI) techniques in die level Microelectronics Failure Analysis (FA) through the IC generations….. *Christian Boit, Technische Universitaet Berlin*
2:30 PM	Break - Regency Terrace			
	Year-in-Review - Regency Main			
3:00 PM	YIR 1: Soft Error in Planar, FDSOI, FinFET and GAA *Taiki Uemura, Samsung Electronics*			
3:50 PM	YIR 2: Advances in Reliability Testing and Understanding for SiC Vertical Power MOSFETs *Daniel Lichtenwalner, Wolfspeed*			
4:40 PM	YIR 3: FEOL Reliability of fin, NW, NS FETs *Erik Bury, imec*			
5:30 PM	Adjourn			

2023 IEEE International Reliability Physics Symposium (IRPS) & International Electrostatic Discharge Workshop (IEW)

Technical Program-at-a-Glance

March 26-30 | Monterey, California, USA

Tuesday • March 28

Time	Min	Regency Main			
8:00 AM	15	General Chair: Welcome & Introduction			
8:15 AM	10	Program Chair: Overview of Technical Program			
8:25 AM	10	Awards			
8:35 AM	50	Keynote 1: Ann Kelleher, Intel			
9:25 AM	50	Keynote 2: Gary Hicok, NVIDIA			
10:15 AM	20	Break - Regency Terrace			
		Regency Main	**Regency I-II-III**	**Regency IV-V-VI**	**Windjammer I**
		2A - GD	2B - NC	2C - GaN	IEW
10:35 AM	5				
10:40 AM	25	2A.1	2B.1	2C.1	IEW Keynote 1 S. Chowdhury
11:05 AM	25	2A.2	2B.2	2C.2	
11:30 AM	25	2A.3	2B.3	2C.3	IEW Keynote 2 M. Shrivastava
11:55 AM	25	2A.4	2B.4	2C.4	
12:20 PM	20	Authors' Corner / Break - Regency Terrace			

12:00 PM - 1:30 PM · Lunch · Monterey Ballroom Sponsored by Synopsys

Time	Min	3A - MR	3B - SiC	3C - PK	IEW
1:25 PM	5				
1:30 PM	25	3A.1	3B.1	3C.1	1:40pm-3:45pm Outdoor Networking Activity Part I
1:55 PM	25	3A.2	3B.2	3C.2	
2:20 PM	25	3A.3	3B.3	3C.3	
2:45 PM	25	3A.4	3B.4	3C.4	
3:10 PM	25		3B.5 - ESREF BP		
3:35 PM	15	Authors' Corner / Break - Regency Terrace			
		4A - EM	4B - CR	4C - GD	IEW
3:50 PM	5				
3:55 PM	25	4A.1	4B.1	4C.1	3:50pm - 5:50pm Outdoor Networking Activity Part II
4:20 PM	25	4A.2	4B.2	4C.2	
4:45 PM	25	4A.3	4B.3	4C.3	
5:10 PM	25	4A.4 - IIRW BSP	4B.4	4C.4 - Late News	
5:35 PM	15	Authors' Corner			
5:50 PM		Adjourn			
6:00 PM	90	Workshop Reception - Mark Thomas Foyer			
7:30 PM	60	Workshops 1-5 & IRDS I			
8:30 PM	15	Break			
8:45 PM	60	Workshops 6-10 & IRDS II			

*workshops available to on-site attendees only

*Invited Speaker

Wednesday • March 29

Time	Min	Regency Main			
8:00 AM	50	Keynote 3: Mark Fuselier, AMD			
8:50 AM	20	Break - Regency Terrace			
		Regency Main	**Regency I-II-III**	**Regency IV-V-VI**	**Windjammer I**
		5A - EL	5B - PI	5C - SR	IEW
9:10 AM	5				
9:15 AM	25	5A.1	5B.1	5C.1	
9:40 AM	25	5A.2	5B.2	5C.2	
10:05 AM	25	5A.3	5B.3	5C.3	
10:30 AM	20	Authors' Corner / Break - Regency Terrace			
		6A - EM	6B - PK	6C - GaN	IEW
10:50 AM	5				
10:55 AM	25	6A.1	6B.1	6C.1	
11:20 AM	25	6A.2	6B.2	6C.2	Seminar + WS 1 ESD Design for high-speed IOs
11:45 AM	25	6A.3		6C.3	
12:10 PM	25	6A.4		6C.4	
12:35 PM	20	Authors' Corner / Break - Regency Terrace			

12:00 PM - 1:30 PM · Lunch · Monterey Ballroom

Time	Min	7A - CR	7B - RT	7C - RE	IEW
1:40 PM	5				
1:45 PM	25	7A.1	7B.1	7C.1	Seminar + WS2 Advanced FinFET ESD Design
2:10 PM	25	7A.2	7B.2	7C.2	
2:35 PM	25	7A.3		7C.3	
3:00 PM	20	Authors' Corner / Break - Regency Terrace			
		8A - TX	8B - FA	8C - RF	IEW
3:20 PM	5				
3:25 PM	25	8A.1	8B.1	8C.1	Seminar + WS 3 JESD78 Latch-Up User Guide Updates
3:50 PM	25	8A.2	8B.2	8C.2	
4:15 PM	25	8A.3	8B.3	8C.3	
4:40 PM	10		Break - Regency Terrace		
4:50 PM	25	8A.4	8B.4	8C.4	Seminar + WS 3 cont.'d
5:15 PM	25	8A.5	8B.5	8C.5	
5:40 PM	20	Authors' Corner			
6:00 PM		Adjourn			
6:00 PM - 9:00 PM	180	IRPS Poster Reception Monterey Ballroom Sponsored by Qualcomm			

Thursday • March 30

Time	Min	Regency Main			
8:00 AM	50	Keynote 4: Rohit Vidwans, Ampere			
8:50 AM	20	Break - Regency Terrace			
		Regency Main	**Regency I-II-III**	**Regency IV-V-VI**	**Windjammer I**
		9A - RT	9B - RE	9C - PI	IEW
9:10 AM	5				
9:15 AM	25	9A.1	9B.1	9C.1	Seminar + WS 4 tAMR (Absolute Maximum Rating)
9:40 AM	25	9A.2	9B.2	9C.2	
10:05 AM	25	9A.3 - Late News	9B.3		
10:30 AM	20	Authors' Corner / Break - Regency Terrace			
		10A - TX	10B - NC	10C - MR	IEW
10:50 AM	5				
10:55 AM	25	10A.1	10B.1	10C.1	IEW + IRPS Posters
11:20 AM	25	10A.2	10B.2	10C.2	
11:45 AM	25	10A.3	10B.3	10C.3	
12:10 PM	25	10A.4	10B.4	10C.4	
12:35 PM	20	Authors' Corner / Break - Regency Terrace			

12:00 PM - 1:30 PM · Lunch · Monterey Ballroom

Time	Min	11A - SiC	11B - MB	11C - PR	IEW
1:40 PM	5				
1:45 PM	25	11A.1	11B.1		Seminar + WS 5 Automotive System-Level
2:10 PM	25	11A.2	11B.2	11C.2	
2:35 PM	25	11A.3	11B.3	11C.3	
3:00 PM	10		Break - Regency Terrace		
3:10 PM	25	11A.4	11B.4	11C.4	Seminar + WS 5 cont.'d
3:35 PM	25	11A.5	11B.5		
4:00 PM	20	Authors' Corner / Break - Regency Terrace			
		Regency Main			
4:20 PM	15	Closing Ceremony, Prize Drawing & 2024 Introduction			
4:35 PM		Adjourn			

Legend

CR - Circuit Reliability and Aging
EM - Emerging Memory
EL - ESD and Latchup
FA - Failure Analysis
GaN - GaN Power Device
GD - Gate/MOL Dielectrics
MR - Memory Reliability
MB - Metal/BEOL Reliability
NC - Neuromorphic Comput. Rel.
PK - Packaging & 2.5/3D Assembly
PI - Process Integration
PR - Product Reliability
RT - Reliability Testing
RE - Radiation Effect Reliability
RF - RF/mmW/5G
SR - System Electronics Reliability
TX - Transistors
SiC - Wide-Bandgap Semi. (SiC)

2023 IEEE International Reliability Physics Symposium (IRPS 2023)

Sunday, March 26

Tutorial 1
Sunday, March 26, 09:00 a.m. – 10:30 a.m. PDT
Venue: Regency Main

09:00 a.m.
TuT1 (Tutorial) - Introduction to Reliability Physics and Engineering, Joe McPherson; McPherson Reliability Consulting LLC

All materials and devices tend to degrade with time. For this reason, reliability physics is of great theoretical and practical importance. Reliability investigations generally start with measuring the degradation rate for a material/device under stress and then a modeling of the time-to-failure versus the applied stress. The term stress, as used here, is very general: stress will refer to any external agent (electrical, mechanical, chemical, thermal, electrochemical, etc.) that is capable of producing material/device degradation. Time-to-failure occurs when the amount of degradation reaches some critical threshold level. Since devices often require different levels of degradation to induce failure, time-to-failure becomes statistical in nature and two common failure distributions are discussed: Weibull and Lognormal. Time-to-failure (TF) modeling generally assumes either a power law or exponential stress-dependence with either an Arrhenius or Eyring-like activation energy. From these TF models, acceleration factors can be deduced and these tend to serve as the foundation for accelerated testing. During this presentation, several semiconductor failure mechanisms will be reviewed: Electro-Migration (EM), Stress Migration (SM), Time-Dependent Dielectric Breakdown (TDDB), Hot-Carrier Injection (HCI), Negative-Biased Temperature Instability (NBTI), Plasma-Induced Damage (PID), Single-Event Upsets (SEU), Surface Inversion, Thermal Cycling Fatigue, and Corrosion. This tutorial should provide the attendee with a solid foundation for a better understanding of the papers presented at the IRPS.

Tutorial 2
Sunday, March 26, 09:00 a.m. – 10:30 a.m. PDT
Venue: Regency I-II-III

09:00 a.m.
TuT2 (Tutorial) - Machine Learning for Integrated Circuit and Semiconductor Device Reliability Analysis, Elyse Rosenbaum; University of Illinois at Urbana-Champaign

All materials and devices tend to degrade with time. For this reason, reliability physics is of great theoretical and practical importance. Reliability investigations generally start with measuring the degradation rate for a material/device under stress and then a modeling of the time-to-failure versus the applied stress. The term stress, as used here, is very general: stress will refer to any external agent (electrical, mechanical, chemical, thermal, electrochemical, etc.) that is capable of producing material/device degradation. Time-to-failure occurs when the amount of degradation reaches some critical threshold level. Since devices often require different levels of degradation to induce failure, time-to-failure becomes statistical in nature and two common failure distributions are discussed: Weibull and Lognormal. Time-to-failure (TF) modeling generally assumes either a power law or exponential stress-dependence with either an Arrhenius or Eyring-like activation energy. From these TF models, acceleration factors can be deduced and these tend to serve as the foundation for accelerated testing. During this presentation, several semiconductor failure mechanisms will be reviewed: Electro-Migration (EM), Stress

Migration (SM), Time-Dependent Dielectric Breakdown (TDDB), Hot-Carrier Injection (HCI), Negative-Biased Temperature Instability (NBTI), Plasma-Induced Damage (PID), Single-Event Upsets (SEU), Surface Inversion, Thermal Cycling Fatigue, and Corrosion. This tutorial should provide the attendee with a solid foundation for a better understanding of the papers presented at the IRPS.

Tutorial 3
Sunday, March 26, 09:00 a.m. – 10:30 a.m. PDT
Venue: Regency IV-V-VI

09:00 a.m.
TuT3 (Tutorial) - BEOL and MOL Reliability, Shinji Yokogawa; The University of Electro-Communications

BEOL reliability has played an essential role in semiconductor technologies, from development to quality assurance. Typical wear-out mechanisms include Electromigration (EM), Stress migration/stress-induced voiding (SM/SIV), Thermo-mechanical stability, and time-dependent dielectric breakdown (TDDB). Recently, reliability issues around gate/contacts, or MOL reliability, have been added to the list. Interconnect, via, and contact reliability challenges caused by defects in and at the metal and dielectrics interface, and their generation, are recognized as important issues, even as generations, structures, and materials change. Understanding them and how to suppress them are the key to achieving high reliability. It is also essential to understand the behavior of the lifetime distribution of each integrated circuit to determine the reliability of integrated circuits, which are made up of many segments. This tutorial will present the physical and statistical fundamentals of these mechanisms. Challenges to BEOL/MOL reliability through new technology miniaturization, material sets, and integration schemes will also be discussed.

Tutorial 4
Sunday, March 26, 09:00 a.m. – 10:30 a.m. PDT
Venue: Big Sur

09:00 a.m.
TuT4 (Tutorial) - LDMOS Reliability: Mechanisms, Methods and Challenges, Guido Sasse; NXP

LDMOS (lateral double-diffused MOS) transistors are essential components in many mixed-signal and RF applications and are used for their high voltage and power handling capabilities. LDMOS transistors are designed such that they exhibit a large breakdown voltage between drain and source while keeping a low on resistance. To achieve this, LDMOS transistors are designed as asymmetric devices with a lightly-doped region near the drain. Typical operating voltages for LDMOS transistors range from 5V and below up to several 100 V. While there are many similarities with baseline CMOS devices in terms of device reliability, the different architecture and different operating conditions, make that LDMOS transistors have various specific reliability concerns. In this tutorial, we will discuss the basic fundamentals of the LDMOS transistor architecture as well as the relevant wear-out mechanisms affecting device reliability. We will also discuss the similarities and differences with baseline CMOS reliability characterization. Furthermore, in this tutorial the methods, and challenges, to assess the lifetime of LDMOS transistors will be discussed.

Break
Sunday, March 26, 10:30 a.m. – 11:00 a.m. PDT

Tutorial 5
Sunday, March 26, 11:00 a.m. – 12:30 a.m. PDT
Venue: Regency Main

11:00 a.m.
TuT5 (Tutorial) - FEOL Reliability in Advanced CMOS Nodes, Yi Zhao; Zhejiang University, Pei Jean Liao; TSMC

Continuous CMOS scaling has been accelerating semiconductor evolution for past years, which makes reliability become one of the most critical segments to enable the technology advancement. Today, advanced Logic technologies are the key drivers for Mobile and HPC segments which empowers innovations to enrich our life. However, new physical reliability studies were eagerly required for deeply scaled transistor development. Therefore, this tutorial will elaborate key FEOL reliability mechanisms including time-dependent dielectric breakdown (TDDB), bias temperature stability (BTI), self-heat effect (SHE) and the reliability risk in cascode configuration design. Furthermore, we will address indispensable plasma induced damage (PID) during process period, as well as the risk to degrade transistor performance and gate dielectrics. Time dependent junction degradation (TDJD) is also covered in this tutorial. Moving toward to leading edge technologies, the past conventional methodologies with Logic based bias and failure criterion fall short of enlarging technology envelope on top of meeting field expectation. Also, there has been a circuit application-based qualification approach to offer an accurate assessment on reliability lifetime for all standard and customized usage. The physical based reliability modeling is going to give clear guidance to reserve guard band through IP/chip or system design. Finally, a comprehensive platform with the coverage of "Design for Reliability" has been deployed for different applications which will be a general practice for future technologies.

Tutorial 6
Sunday, March 26, 11:00 a.m. – 12:30 a.m. PDT
Venue: Regency I-II-III

11:00 a.m.
TuT6 (Tutorial) - Impedance Spectroscopy of the MOS Systems, Paul K. Hurley; Tyndall National Institute University College Cork

Impedance spectroscopy of metal-oxide-semiconductor (MOS) systems has been used since the 1960's, as one of the principal experimental methods to characterize and quantify the properties of the MOS system which is at the heart of logic and memory structures. The tutorial will cover the following aspects:

1. The fundamental measurement of impedance (Z) and phase angle (ö), and how this data is transformed into capacitance (C) and conductance (G) by imposing an equivalent circuit topology on the device under test.
2. The significance and applications of using a series and/or a parallel circuit topology.
3. The universal relationship between C and G through the Kramers-Kronig equation, and its applications.
4. The emergence of MOS systems not dominated by interface defects, with examples of III-V MOS and MOS systems formed on 2 D semiconductors.
5. The use of non-local phonon-assisted tunneling to traps to characterize the oxide defect density as a function of space and energy in the InGaAs MOS system.
6. A general method to discriminate between interface and oxide defects in MOS structures.
7. Impedance spectroscopy of metal-oxide-semiconductor (MOS) at cryogenic temperatures. Do defects still respond?

Tutorial 7
Sunday, March 26, 11:00 a.m. – 12:30 a.m. PDT
Venue: Regency IV-V-VI

11:00 a.m.
TuT7 (Tutorial) - Various Reliability Issues in DRAM Cell Transistors, Junsoo Kim; Samsung

As the DRAM cell transistor has been increasingly scaled, various reliability concerns have emerged. The read, write, and retention of data are the three main functions of the DRAM cell transistor. Each operation mode has its own issues. Usually, memory chips are pre-screened and repaired before and after packaging. Nevertheless, some reliability measures such as VRT (variable retention time) or Row hammer (an issue of interaction electrically between memory cells by leaking their charges) are difficult to screen, because it is not triggered by thermal or electric field. And suppressing of single event effect contributed by thermal neutrons from cosmic-ray is also necessary to assure the reliability of DRAM chips. In this tutorial, a comprehensive understanding of classic items and recent challenges including soft errors induced cosmic-ray at ground level is presented.

Tutorial 8
Sunday, March 26, 11:00 a.m. – 12:30 a.m. PDT
Venue: Big Sur

11:00 a.m.
TuT8 (Tutorial) - RRAM Based AI and Reliability, J. Joshua Yang; University of Southern California

In the era of 'big data' and 'Internet of Things', the traditional computing architecture based on CMOS hardware has become increasingly inefficient to support Artificial Intelligence (AI) and Machine Learning (ML), which necessitates some emerging technologies, such as RRAM technology (also called memristors when dynamical properties are emphasized). RRAM technology was initially developed for the next-generation nonvolatile memories, for which there are still some remaining challenges to be overcome before a large-scale commercialization is feasible. On the other hand, computing applications are less constrained by such challenges and represent low-hanging fruits for its applications. I will first introduce the state of the art of these devices and how they are used for AI and ML. I will then focus on the challenges and possible solutions for those devices when they are used for AI, with the reliability issue being highlighted.

Break
Sunday, March 26, 12:30 p.m. – 01:30 p.m. PDT

Tutorial 9
Sunday, March 26, 01:30 p.m. – 03:00 p.m. PDT
Venue: Regency Main

01:30 p.m.
TuT9 (Tutorial) - BTI in Advanced HKMG for Future CMOS Tech Nodes, Jacopo Franco; imec

Negative Bias Temperature Instability (NBTI) has been a primary reliability concern since the early days of Si MOS technology. Decades later, the introduction of high-k dielectrics expanded the concern also towards n-channel devices, with Positive BTI becoming a comparable concern. We will review the basics of BTI, in terms of phenomenology, characterization techniques and proposed models. Next, we will focus on specific BTI challenges in upcoming CMOS technology nodes. In particular, the introduction of nanosheet device architectures with tight vertical pitches, and of stacked device concepts such as the Complementary FET (CFET) are expected to complicate the deployment of common BTI optimization strategies based on sacrificial gate caps and high temperature anneals. Furthermore, the continuously increasing complexity of multi-Vth device offering, comprising a wider range of gate work function metal stacks, might expose additional dielectric defect levels whose role might have been neglected so far. We will highlight the importance of identifying the microscopic defect structures responsible for

each BTI signature in advanced gate stacks, in order to successfully develop novel targeted BTI treatments within ever more stringent fabrication constraints

Tutorial 10
Sunday, March 26, 01:30 p.m. – 03:00 p.m. PDT
Venue: Regency I-II-III

01:30 p.m.
TuT10 (Tutorial) - Emerging Memories Reliability: From Device to Applications, Cristian Zambelli; University of Ferrara

Emerging memory technologies such as Resistive Switching Memories (RRAM), Phase Change Memory (PCM) and Magnetic RAM (MRAM) are disrupting the storage hierarchy by offering performance metrics at the intersection of DRAMs (used as main working memory in almost all computer architecture) and NAND Flash (the core of bulk storage systems such as Solid-State Drives). A considerable number of embedded and high-performance computing (HPC) systems are envisioning the adoption of these Storage Class Memories (SCM) in their designs to improve latency, throughput, and power consumption figures. In addition, by arranging such revolutionary memory cell concepts in crossbar array topologies, we testify unprecedented integration scenario such as neuromorphic and in-memory computing, thus enabling energy-efficient non-Von Neumann architectures. The path towards the commercialization of emerging memory technologies is however strictly dependent on the reliability features offered both on the short-term (disturbs and read/write stability) and on the long-term (endurance and data retention). In this tutorial, we will address three technologies in the landscape of the emerging memories by showing how their physical working principles and their integration characteristics pose significant reliability threats that must be mitigated either with a careful device engineering or with a system-level approach. A link between the reliability figures of merit and the application scenario foreseen for each technology is explored throughout the entire tutorial.

Tutorial 11
Sunday, March 26, 01:30 p.m. – 03:00 p.m. PDT
Venue: Regency IV-V-VI

01:30 p.m.
TuT11 (Tutorial) - Heterogenous Integration Reliability Challenges and Roadmap, Richard Rao; Marvell Technology

This tutorial examines the reliability implications of 'SysMoore', i.e. system-level heterogeneous integration (HI), that is being developed as a means to keep delivering the rate of performance increase, that we have come to expect because of Moore's Law. Increasing system complexity, functionality, diversity, and density, as a result of the twin drives for HI and on-chip advances, will pose new challenges for meeting and verifying customers' reliability targets. Multifunctional HI systems of the future are expected be complex multiscale and multiphysics systems. Heterogeneous integration requires a convergence between the semiconductor industry and the packaging industry, and a unified reliability approach across the entire product architecture hierarchy from device level to package, boards/ modules, and systems. The resulting complex chip-package-board interactions (CPBI) will pose new reliability challenges and will need to be addressed by an integrated reliability team across all these levels of device-to-system integration, to meet the customer's reliability targets. HI reliability engineers will also need to meet holistic constraints such as reducing the time required for new product introduction (NPI) and minimizing cost of ownership over the life-cycle of successive generations of products. Such an integrated approach towards reliability will require a rigorous, disciplined, and proactive fusion approach that strategically combines a bottom-up reliability physics approach with a top-down approach that leverages powerful artificial intelligence algorithms and the unprecedented levels of real-time field performance data, service condition data, product stress data and

system/component reliability data that is becoming available via IoT infrastructure. This tutorial lays out the scope, challenges, disruptive opportunities, and potential approaches for achieving such an integrated reliability approach for HI technologies that are likely to emerge over the next 0-5, 5-10 and 10-15 years.

This tutorial will focus on the following aspects of heterogenous integration reliability.

1. Introduction of heterogenous integration packages such as chiplet, 2.5D and 3D package integrations.
2. Reliability failure modes and degradation mechanisms for multi-level interconnects in the heterogenous integration system such as TSV, uBumps, RDLs and hybrid bonding, etc.
3. Chip package and board integrations
4. Design for reliability
5. Qualification for reliability

Tutorial 12
Sunday, March 26, 01:30 p.m. – 03:00 p.m. PDT
Venue: Big Sur

01:30 p.m.
TuT12 (Tutorial) - MEMS Reliability, Ashwin Seshia; Cambridge University

Microelectromechanical systems (MEMS) technology has made rapid strides in addressing large volume as well as niche applications such as physical and chemical sensors, timing and frequency control, and component technologies for radio frequency communication systems. Microelectromechanical devices are fabricated using semiconductor batch manufacturing techniques and often consist of electrically interfaced moving parts on a silicon chip, introducing additional criteria for reliability assessment. This tutorial will cover an overview of the physical mechanisms underpinning performance degradation and failure in microelectromechanical systems while maintaining a focus on free standing silicon-based microelectromechanical devices. Physical models underpinning the behaviour of specific types of devices will be introduced including (1) inertial sensors, (2) resonators, and (3) vibration energy harvesters. Aspects relating to performance over temperature/temperature cycling, shock and vibration loading, and other environmental conditions will be covered. A discussion of various approaches to address the development of high yielding, high-performance parts developed at the device, process, assembly and packaging, and system integration levels will be discussed.

Break
Sunday, March 26, 03:00 p.m. – 03:30 p.m. PDT

Tutorial 13
Sunday, March 26, 03:30 p.m. – 05:00 p.m. PDT
Venue: Regency Main

03:30 p.m.
TuT13 (Tutorial) - Reliability Characterization of CMOS Ring Oscillator Circuits in Scaled CMOS Technologies, Andreas Kerber; Intel

Reliability characterization of CMOS technologies is primarily focused on bias temperature instability (BTI), hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) using discrete devices. In recent years, characterization methods were extended from DC to AC waveforms to better capture the widely discussed recovery effects and to assess lifetime under switching conditions mimicking digital operation.

In this tutorial we focus on reliability characterization of CMOS ring-oscillators (RO) circuits representing a

fundamental digital circuit block. We discuss time resolved RO frequency measurements and its importance in capturing the BTI component in digital circuit aging. We identify HCI contributions in RO by varying test temperature and using different test structure designs. We also address the relevance of self-heating and attempt to correlate the aging in discrete devices to degradation in ROs in scaled CMOS technologies.

Tutorial 14
Sunday, March 26, 03:30 p.m. – 05:00 p.m. PDT
Venue: Regency I-II-III

03:30 p.m.
TuT14 (Tutorial) - Design for Reliability in Product Development, Ranjani Muthiah; Google

A systematic, proactive approach to product reliability is essential to deliver highly reliable products. This tutorial will outline the components of a Design for Reliability program that is key for successful Product Development. Methodologies used in product design and manufacturing for reliability in Photonic ICs will be reviewed. Accelerated stress testing strategies and their applicability to field use conditions will be discussed. Details and considerations for reliability in product development, with examples from highly reliable Photonic Integrated Circuits, will be presented.

Tutorial 15
Sunday, March 26, 03:30 p.m. – 05:00 p.m. PDT
Venue: Regency IV-V-VI

03:30 p.m.
TuT15 (Tutorial) - Reliability Challenges for Si Photonics Products, Arif Zaman, Quan Tran; Intel

Intel's Silicon Photonics (SiP) program overview will be provided. Next, reliability challenges and qualification methodology of SiP components are discussed. In particular, the challenges in qualification of those components for integrating them into LiDAR application are addressed. Finally, the methodology to qualify optical transceiver products with integrated SiP components is presented.

Tutorial 16
Monday, March 26, 03:30 p.m. – 05:00 p.m. PDT
Venue: Big Sur

03:30 p.m.
TuT16 (Tutorial) - Reliability of Encapsulating Molding Compounds for Electronic Packaging Subjected to High Field and Different Environmental Conditions, Susanna Reggiani; University of Bologna

The study of physical properties of encapsulation materials used in power electronic industry has raised increasing interest in recent years, as package design is a key aspect in device reliability. Polymeric molding compounds are known to be source of surface charging effects, mainly attributed to dielectric losses, ionic conductivity and charge accumulation at the interface with the passivation layers. The understanding of charge spreading is of primary importance to improve device reliability at the design stage. Given the technological importance, a number of novel characterization methods have been recently proposed. Among them, low-field conductivity, dielectric spectroscopy and pulsed electro-acoustic characterizations have been implemented on bulk samples, while special test chips with integrated charge sensors allowed for the characterization of the lateral charge spreading in more realistic operating conditions. Special fucus has been devoted to environments with high humidity conditions showing significant changes in the dielectric properties. Numerical simulations based on commercial TCAD tools were also carried out with the purpose of a deeper physical insight. High-voltage lateral devices like, e.g., LDMOS

transistors or GaN HEMTs, are expected to be strongly impacted by mobile charges on the overlying isolation. In this tutorial, an investigation of the package-induced effects will be addressed by reviewing the main features of polymers, their numerical simulation and their characterization at different conditions.

Monday, March 27

Tutorial 17
Monday, March 27, 08:30 a.m. – 10:00 a.m. PDT
Venue: Regency Main

08:30 a.m.
TuT17 (Tutorial) - Device and Interconnect Reliability Implications for Digital and Analog Circuit Design,
Sachin Sapatnekar; University of Minnesota

Reliability problems are a serious issue in modern digital and analog circuits. As design moves to FinFET/GAAFET nodes and beyond, devices and interconnects undergo increasing levels of stress as they carry higher currents (for digital circuits), or prolonged continuous bias currents (for analog circuits), or are subjected to prolonged voltage stresses. This presentation presents an overview of methods for analyzing and optimizing VLSI circuit reliability, going from device modeling approaches to circuit and system optimization at an appropriate level of abstraction for the circuit/system designer. As typical industry design flows find detailed physics-based models to be too complex for practical use, and instead use empirical models that provide fewer insights, recent efforts at the circuit level have attempted to close this gap. For example, for the problem of electromigration (EM) analysis, recent work has reduced the complexity of solving the physics-based equations that model EM, creating credible alternatives to empirical methods. The focus of this tutorial is on providing the link between physics-based models for bias temperature, hot-carrier injection, time-dependent dielectric breakdown, and electro migration, and their deployment into simulation and optimization techniques at the chip or system level, for both digital and analog systems.

Tutorial 18
Monday, March 27, 08:30 a.m. – 10:00 a.m. PDT
Venue: Regency I-II-III

08:30 a.m.
TuT18 (Tutorial) - The Role of Defects in the Dynamic Lifetime of GaN Power Devices, Clemens Ostermaier; Infineon Technologies

Gallium nitride (GaN) offers fundamental advantages over silicon. In particular the higher critical electrical field makes it very attractive for power semiconductor devices with outstanding specific dynamic on-state resistance and smaller capacitances compared to silicon switches, which makes GaN HEMTs great for high speed switching.

Besides the polarization charge induced 2-dimensional electron gas, two key defects control the device behavior: Interface defect states controlling the electron concentration in the lateral device channel and deep defect states in the buffer enabling the vertical buffer insulation.

This tutorial aims to review the latest understanding of those device behavior defining defects and look further into their role in lifetime limiting robustness issues of GaN devices under dynamic switching conditions. A particular focus will be effects of hot carriers trapping in the device during hard-switching stress conditions leading a steady increase in dynamic on-resistance and also hard failures.

Tutorial 19
Monday, March 27, 08:30 a.m. – 10:00 a.m. PDT
Venue: Regency IV-V-VI

08:30 a.m.
TuT19 (Tutorial) - Radiation Effects in a Post-Moore World, Dan Fleetwood; Vanderbilt University

In this tutorial a number of milestones in the evolution and understanding of total-ionizing-dose and single-event effects are reviewed within the context of classical Dennard scaling. The discussion will focus on the discovery of fundamental mechanisms, development of radiation-tolerant IC technology, and increasing maturity and complexity of Si-MOS-based devices, circuits, and systems. Examples are shown that illustrate how the end of Dennard scaling has influenced radiation effects in current technology generations, due to the increasingly complex and diverse materials and devices that are now incorporated. The radiation responses of devices with alternative channels to silicon and transistors based on 2-D materials are discussed, with an emphasis on the mechanisms of defect formation. The utility of low-frequency (1/f) noise measurements in defect characterization will be discussed within this context. In the future, many types of microelectronic devices and ICs will become more vulnerable to radiation effects and more difficult to test in a practical and cost-effective manner. This will become an ongoing challenge for the international radiation effects community, particularly for ultimately scaled devices and/or quantum computing.

Tutorial 20
Monday, March 27, 08:30 a.m. – 10:00 a.m. PDT
Venue: Big Sur

08:30 a.m.
TuT20 (Tutorial) - Reliability and Variability of CMOS Devices at Cryogenic Temperatures, Alexander Grill; imec

Integrating CMOS circuits and qubits at cryogenic temperatures is one of the key challenges to mitigate wiring constraints and ensure signal integrity to enable up-scaling of quantum computers. While operating in the GHz-regime, interfaces between classical and quantum circuits need to maintain ultra-low power consumption together with very low noise figures. One approach to reduce power consumption is to optimize designs towards operation at lower supply voltages. However, this also reduces the tolerable margins on variability, parameter drift, and device to device variations.

In this tutorial, I will present an overview on the physics of cryo-CMOS devices with a special focus on device variability and reliability. I will present our current understanding of low-frequency noise and modelling of charge trapping kinetics at cryogenic temperatures. I will also highlight the importance of integrated metrology structures to overcome the measurement bottleneck arising in most common cryogenic probers.

Break
Monday, March 27, 10:00 a.m. – 10:30 a.m. PDT

Tutorial 21
Monday, March 27, 10:30 a.m. – 12:00 p.m. PDT
Venue: Regency Main

10:30 a.m.
TuT21 (Tutorial) - Physical Modeling of Reliability Challenges in SiC Power Devices, Michael Waltl; Institute for Microelectronics, TU Wien

Transistors employing silicon carbide (SiC) substrates exhibit excellent electrical properties for high-voltage power conversion applications. In particular, a lot of effort has been put into the development of SiC metal-oxide-semiconductor (MOS) transistors as they provide a much lower specific on-resistance for a given blocking voltage and can operate at higher temperatures compared to conventional Si transistors. The advantages of SiC-based MOS transistors arise from the superior properties of SiC, such as high breakdown voltage, large bandgap, and high thermal conductivity.

State-of-the-art SiC power MOSFETs mostly use a vertical device architecture which has the advantage of having a high blocking voltage and comparable small on-resistance, maintaining a small chip area compared to lateral device structures. Besides these major advantages, vertical SiC MOSFETs exhibit higher carrier mobility due to reduced trap density in the vicinity of the conduction band edge, but larger defect densities within the SiC bandgap. To passivate as many of these defects as possible various post-oxidation anneals have been studied in the past. But still, a considerable number of traps remain, which are the central origin for dynamic changes e.g. in the threshold voltage, which becomes visible as hysteresis of voltage sweep measurement and experiments performed to investigate bias temperature instabilities. It has to be noted that the physical understanding and modeling of the defects and their impact on the devices is vital to enable studying device performance degradation and its impact on the behavior of circuits. In this talk, an overview of reliability challenges and recent advances in SiC power MOSFETs is given. Also, the latest modeling efforts toward a consistent explanation of device electrostatics, e.g. the simulation of IV sweeps, but also the explanation of transient effects by means of TCAD simulations, are addressed. Finally, based on the calibrated simulations, the model parameters can be linked to certain trap candidates. However, for the SiC material system, there is a large variety of potential trap candidates available that might contribute to charge trapping.

Tutorial 22
Monday, March 27, 10:30 a.m. – 12:00 p.m. PDT
Venue: Regency I-II-III

10:30 a.m.
TuT22 (Tutorial) - Automotive Electronics Reliability – Challenges and Opportunities, Pradeep Lall; Auburn University

The modern car has increased semiconductor content and dollar value. Semiconductors enable the majority of innovations in automotive. The increased emphasis on autonomous driving and the electrification of vehicles has resulted in enormous changes for semiconductors and packaging. The design, materials, and reliability strategies for automotive electronics will be presented. Electronics are increasingly being used in automotive platforms for various mission-critical and safety-critical activities, such as guidance, navigation, control, charging, sensing, and operator interaction. Over the last two decades, automotive platforms have expanded to incorporate hybrid and fully-electric vehicles. Much of the electronics is located under the car's hood or in the trunk, where temperatures and vibration levels are far higher than in consumer office applications. During the vehicle's use-life, electronics in the automotive underhood may be exposed to sustained high temperatures of 125-150°C for extended periods of time. The automotive electronics council (AEC) has graded electronics for automotive purposes into four categories: grade-0, grade-1, grade-2, and grade-3. Grade-0 components have the most demanding criteria of the four grade categories, with predicted power temperature cycling ranging from -40°C to +150°C for 1000 cycles and ambient temperature cycling ranging from -55°C to +150°C for 2000 cycles. Furthermore, the grade-0 components are expected to be capable of sustaining high-temperature storage for 1000 hours at 175°C. With the introduction of new packaging architectures, packaging applications have continued to evolve, allowing for powerful computing

on mobile automobile platforms. New materials and integration technologies have also emerged, allowing for tighter integration of electronics sensing and processing into the structural characteristics of the vehicle. The automobile platform faces a series of constraints particular to the real-time context for enabling sophisticated functionality.

Tutorial 23
Monday, March 27, 10:30 a.m. – 12:00 p.m. PDT
Venue: Regency IV-V-VI

10:30 a.m.
TuT23 (Tutorial) - Soft Errors – From Simple Devices to Complex Systems, Indranil Chatterjee; Airbus

With diminishing feature sizes, radiation effects in semiconductor devices continue to be the dominant failure mechanism compared to all other "hard" reliability failure modes combined. With the push to deploy data-intensive edge-computing applications, be it in aircraft, satellites, or autonomous vehicles, soft-errors have a strong impact on system reliability, dependability, and availability. These applications use commercially available high-performance components which do not use any Radiation-Hardening-by-Design (RHBD) concepts and Size, Weight, and Power (SWaP) are the key metrics, making them susceptible to radiation induced faults. Thus, system-level handling and mitigation of soft errors is imperative for successful deployment of these components in radiation environments.

In this short course, an overview of the single-event effects impacting advanced semiconductor nodes will be discussed. Key metrics for designing SEE tests, such as sample preparation, biasing conditions, thermal impacts, internal fault tolerance mechanisms, etc. will be covered. Being able to determine the interplay of these variables is an integral part of designing a test to meet the needs of a specific application. Efficacies and limitations of board-level SEE testing, as opposed to component-level SEE testing, will also be discussed. Finally, the course will focus on the system level aspects of soft errors, and provide a global overview of how complex systems such as autonomous vehicles, aircraft, or satellites handle soft errors, and, ensure performance and reliability in various application environments, from ground to space.

Tutorial 24
Monday, March 27, 10:30 a.m. – 12:00 p.m. PDT
Venue: Big Sur

10:30 a.m.
TuT24 (Tutorial) - Reliability of Semiconductor Spin Qubits for Quantum Computing, Michael Jura; HRL Laboratories

Over the past two decades significant progress has been made using spins in semiconductors as qubits for quantum computing, yet semiconductor qubits currently trail other architectures (including those utilizing superconductors or trapped ions) in number of demonstrated qubits. No architecture has yet achieved the number of qubits needed to reach the promise of quantum computing, and semiconducting qubits' potential lies in the ability to scale more rapidly, both in terms of quantum-coherent control and fabrication. In this tutorial, we review gate-defined semiconductor spin qubits and discuss yield and reliability concerns that are unique to the technology, as well as those common with CMOS integrated circuits. We consider the demands for spin qubits applied to device and process design and process control. We review the fabrication and operation of major types of spin qubits, including donor spin qubits, single-spin "Loss-DiVincenzo" qubits, and triple-spin exchange-only qubits. We next discuss device yield failure mechanisms at quantum-relevant temperatures (typically ~0.1 K) such as poor gate connectivity, poor signal delivery, electrostatic disorder (similar to threshold uniformity), charge noise, magnetic noise, and accessibility of excited quantum states. Reliability issues include threshold drift, repeated thermal cycling, and

electrostatic discharge. Finally, we discuss HRL's approach to reliable quantum technology: the SLEDGE (single-layer etch-defined gate electrode) platform.

Break
Monday, March 27, 12:00 p.m. – 01:00 p.m. PDT

Tutorial 25
Monday, March 27, 01:00 p.m. – 02:30 p.m. PDT
Venue: Regency Main

01:00 p.m.
TuT25 (Tutorial) - Insulators for Devices Based on 2D Materials, Tibor Grasser; TU Vienna

Despite the breathtaking progress already achieved for 2D electronic devices, they are still far from exploiting their predicted performance potential. This is in part due to the lack of scalable insulators, which would go along with 2D materials as nicely as SiO2 goes with silicon. As a result, there is still no commercially competitive 2D transistor technology available today.

The selection of suitable insulators for 2D nanoelectronics represents an enormous challenge. However, this problem is of key importance, since scaling of 2D semiconductors towards sub-10nm channel lengths is only possible with gate insulators scalable down to sub-1nm equivalent oxide thicknesses (EOT). In order to achieve competitive device performance, these insulators need to meet stringent requirements regarding (i) low gate leakage currents, (ii) low density of interface traps, (iii) low density of border insulator traps and (iv) high dielectric strength.

The insulators typically used for 2D electronic devices are amorphous 3D oxides known from Si technologies (SiO2, HfO2, Al2O3), while native 2D oxides (MO3, WO3 and Bi2SeO5), layered 2D crystals (hBN, mica) and ionic 3D crystals (CaF2 and other fluorides like SrF2, MgF2) have received increasing attention. 3D oxides form poor quality interfaces with 2D semiconductors and contain border traps which severely perturb stable device operation. Native oxides, on the other hand, are often non-stoichiometric due to the lack of well-adjusted oxidation methods and thus have a limited dielectric stability and inherently narrow bandgaps. As the most popular candidate, the layered 2D insulator hBN forms excellent van der Waals interfaces with 2D semiconductors, but has mediocre dielectric properties resulting in excessive leakage currents for sub-1nm EOT. The potential of other 2D insulators (e.g. mica) is currently unclear, in part due to the absence of scalable growth techniques. Finally, very promising insulators for 2D electronics are 3D ionic crystals like CaF2 which form well-defined interfaces to 2D channel materials. In contrast to hBN, fluorides have good dielectric properties and thus exhibit low gate leakage currents. This tutorial will address the current state of the art and summarize the main problems together with potential solutions.

Tutorial 26
Monday, March 27, 01:00 p.m. – 02:30 p.m. PDT
Venue: Regency I-II-III

01:00 p.m.
TuT26 (Tutorial) - Ferroelectric Hafnium Oxide Based FeFETs - Device Reliability for Non-Volatile Memories and Beyond, Stefan Slesazeck; NamLab

The discovery of ferroelectricity in doped hafnium oxide that was firstly published in 2011 by Böschke et al. strongly increased the interest in ferroelectric memory devices. The polarization reversal in these thin films is used to store information in different device types. One of them is the ferroelectric field effect transistor (FeFET). The electrical characteristics of these devices are strongly influenced by the whole device design and material stack, rather than being dictated by the properties of the ferroelectric layer itself. Therefore, in this tutorial, I will first

discuss the fundamental reliability aspects of ferroelectric hafnium oxide. In a second part I will shed some light on the specific reliability aspects of the different FeFET designs for their application in memory arrays and for the realization of unconventional computing paradigms.

Tutorial 27
Monday, March 27, 01:00 p.m. – 02:30 p.m. PDT
Venue: Regency IV-V-VI

01:00 p.m.
TuT27 (Tutorial) - RF Si CMOS and GaN Reliability for 5G/mmWave/RF Applications, Purushothaman Srinivasan; GlobalFoundries, Don Gajewski; Wolfspeed

Si CMOS:
This tutorial will provide a practical overview of the key reliability mechanisms along with the challenges faced by reliability engineers studying the reliability of 5G/WiFi and mmWave/RF applications implemented with silicon-based technologies. This tutorial reviews current progress in our understanding on key impact of short- and long-term stress on key RF metrics and new methodologies for RF reliability estimation in Front-End-Module circuits. The tutorial will also cover (1) Major reliability mechanisms affecting the designs based on waveform analysis 2) Simulation and Modeling behavior under DC and RF conditions including self-heating using industry standard simulators, 3) Approach to the validation of the RF reliability models in silicon, 4) Long term reliability evaluation stress results and lifetime estimation under RF conditions and 5) An engineering approach on how to balance and optimize the Performance/Reliability trade-offs, providing a practical approach to Safe Operating Area will be presented. Throughout this tutorial, several examples of reliability stress data along with the models to support our methodology and conclusions will also be presented.

III-V:
This tutorial will provide an overview of the failure mechanisms, reliability characterization techniques, intrinsic lifetime extrapolations, and qualification strategies for GaN devices for 5G/RF/mmW applications. Failure mechanisms include reverse piezo-electric GaN cracking, source-connected field plate electromigration driven by RF signals, ohmic contact degradation, humidity effects and charge trapping. Reliability characterization techniques include on-state (accelerated life test, DC- and RF-ALT, and high temperature operating life, DC- and RF-HTOL), off-state (high temperature reverse bias, HTRB) and accelerated gate bias. This tutorial will review approaches for constructing reliability and qualification plans for covering the RF I-V plane for various amplifier class modes and harsh operating environments.

Tutorial 28
Monday, March 27, 01:00 p.m. – 02:30 p.m. PDT
Venue: Big Sur

01:00 p.m.
TuT28 (Tutorial) - Contactless Fault Isolation (CFI) Techniques in Die Level Microelectronics Failure Analysis (FA) through the IC Generations from Micro to Nanoscale Nodes and Backside Power Distribution Networks, Christian, Christian Boit; Technische Universitaet Berlin

Contactless fault Isolation (CFI) on ICs started with a wide range of perspectives, from liquid crystal hot spot analysis to E beam probing. Over time, optical techniques became the most successful approaches that became even more established in the IC generations of flip chip and interconnect planarization. Infra red based CFI techniques like Photon Emission, Laser Stimulation inducing Delay Variation and/or Electro-optical probing have been very powerful to track almost each signal in Integrated Circuits.

This enormous success is challenged by the progress in IC technology to node dimensions smaller than 14nm. Resolution can be improved by the use of shorter optical wavelengths but the price is drastical thinning of bulk silicon sub micron level plus a transparent solid immersion lens (SIL) on the top.

In order to have CFI at any node size, a new approach reaching out to e beam probing based on very complex and meticulous preparation techniques is finding its way to meet the needs of single digit nanoscale node size IC technologies.

The tutorial discusses also the critical points: Invasiveness of removal techniques, mechanical and thermal aspects, and how the individual design of a composition of global and local preparation techniques may make all the difference for success. It also presents a vision what fault isolation of an IC with Backside Power Distribution Networks could look like.

Break (All breaks are in the: International Foyer)
Monday, March 27, 02:30 p.m. – 03:00 p.m. PDT

Reliability Year-in-Review
Monday, March 27, 03:00 p.m. – 05:30 p.m. PDT
Venue: Regency Main

03:00 p.m.
YIR1 (Year-in-Review) - Soft Error in Planar, FDSOI, FinFET and GAA, Taiki Uemura; Samsung Electronics

Radiation effect in semiconductor devices is a critical concern in high-performance computing (HPC) and automotive applications. The HPC scale grows more than Moor's law, an HPC system has over 8 million semiconductor devices, and the required quality is extremely high in a semiconductor device. Screening and process modification are not able to prevent soft errors; soft error is the principal concern in HPC reliability. This YIR will cover state-of-the-art of soft error technology in the advanced technology as applied to HPC. Automotive is another application that has a huge concern about soft error. Qualification of automotive devices is compliance with ISO26262 and AEC-Q100. The two standards follow a JEDEC standard, JESD89 (Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices). JESD89 has been updated 2021 (JESD89B), and this YIR explains the update in JESD89. This YIR will cover the new potential radiation effect: X-ray effect and SEFI in DRAM, and SEE in MRAM.

03:50 p.m.
YIR2 (Year-in-Review) - Advances in Reliability Testing and Understanding for SiC Vertical Power MOSFETs, Daniel Lichtenwalner; Wolfspeed

Recent years have seen much focus on the advancement of SiC power devices from niche applications to mainstream power conversion applications. SiC diodes and MOSFETs are key components in power conversion devices and modules for various industrial applications ranging from solar, wind, computer servers, traction, among others. These devices have shown their ability to provide energy efficiency savings due to their low on-state resistance in high voltage applications (typical product offerings range from 650V to 3.3kV), and low switching energy losses. The performance benefits of SiC power devices in efficiency compared to competing silicon-based devices is clear.

The recent push for SiC power MOSFETs in automotive applications (chargers, motor drives) has increased the focus on ensuring low (ppm) failure rates, and consequently demands a more complete understanding of all failure mechanisms. Thus the last few years have seen a multitude of studies aimed to fully characterize the complete

device operating conditions in static and dynamic device operation. Both intrinsic and extrinsic failure modes have been studied in much more detail due to these demands of automotive products and their qualification criteria.

In this review, a summary of the many important reliability tests for SiC MOSFETs will be discussed, explaining differences between silicon and SiC-based devices, and then focusing on threshold stability tests that are critical for SiC MOS devices. Namely, the issue of threshold drift under gate switching (gate switching instability, GSI) has been recently observed to be unlike that experienced in silicon devices, and various studies have been published which elucidate the effects of this failure mode, with some explanation regarding the origins of this failure mechanism. The results presented in these recent studies will be summarized.

04:40 p.m.
YIR3 (Year-in-Review) - FEOL Reliability of Fin, NW, NS FETs, Erik Bury; imec

The arrival of the mobile era and the internet of things requires long battery life for electronic components and low OFF currents. Thus, transistors are optimized by introducing novel device topologies such as fin, nanowire (NW), nanosheet (NS), and forksheet (FS) field-effect-transistors (FETs). They are designed to improve electrostatic channel control and result in a steeper sub-threshold slope and hence an improved ratio between ON and OFF currents. Thereby a reduction of the device power consumption and further scaling of the supply and threshold voltages becomes possible. In addition to such tangible product parameters as performance and power consumption, reliability specifications are the essential metric required for the introduction of each new VLSI node.

In this year-in-review we provide a summary of recent papers devoted to front-end-of-line (FEOL) reliability concerns in fin, NW, NS, and FS FETs: bias temperature instability (BTI), hot-carrier degradation (HCD), OFF-state stress (OSS), and self-heating (SH), as well as their intricate superpositions. This presentation rests on three pillars: (i) experimental investigations of the degradation issues in the novel devices, (ii) strategies on how to alleviate these degradation effects and optimize the device architecture, and (iii) predictive lifetime modeling for FETs subjected to BTI, HCD, OSS, and SH.

Monday, March 28

IRPS Welcome, Program Overview & Awards
Tuesday, March 28, 08:00 a.m. – 08:35 a.m. PDT
Venue: Regency Main

Keynote 1
Tuesday, March 28, 08:35 a.m. – 09:25 a.m. PDT
Venue: Regency Main

08:35 a.m.
KN1 (Keynote) - On the Advance of Moore's Law and Resulting Trends in Reliability, Ann Kelleher; Intel

The semiconductor industry is driving innovation at a Moore's Law cadence to satisfy the world's ever-increasing demand for compute and connectivity. Innovation is driven by customer needs for product functionality, and is enabled by novel transistor, interconnect, memory, and packaging architectures. These innovations across the industry increase system complexity and impact reliability. This keynote discusses future silicon, packaging technologies and reflects upon their implications for the reliability community. The benefits of a System Technology Co-Optimization (STCO) approach for reliably delivering functionality will also be briefly discussed.

Keynote 2
Tuesday, March 28, 09:25 a.m. – 10:15 a.m. PDT
Venue: Regency Main

09:25 a.m.
KN2 (Keynote) - Transforming Industries with Trustworthy Cloud-to-Edge Compute Platforms, Gary Hicok; Nvidia

Advanced computing systems are beginning to be used in critical life-saving applications. High-performance solutions are transforming transportation, medical and other vital information technology systems, along with drug discovery, climate research and more. Trusting these systems, which are composed of silicon, hardware, software and reliant on a huge amount of data, has become essential to success. This trust is primarily built on reliability, safety and security.

Along with the rising need for trustworthiness, platforms themselves are advancing, becoming more complex and scalable. They extend from the cloud to high-performance embedded systems with hybrid systems-of-systems that feature parts of each. This new unit of computing opens up more potential for failure, but also affords more opportunities to improve trust by cross-utilizing hardware, software and system techniques. This talk covers cross-discipline and cross-system approaches to check, monitor, predict, protect, deliver redundancy and simulate end-to-end compute platform trustworthiness.

Break
Tuesday, March 28, 10:15 a.m. – 10:35 a.m. PDT

2A – GD (Gate/MOL Dielectrics)
Tuesday, March 28, 10:35 a.m. – 12:20 p.m. PDT
Venue: Regency Main

10:40 a.m.
2A.1 - Investigating Nanowire, Nanosheet and Forksheet FET Hot-Carrier Reliability via TCAD Simulations, Michiel Vandemaele, Ben Kaczer, Erik Bury, Jacopo Franco, Adrian Chasin, Alexander Makarov, Hans Mertens, Geert Hellings, Guido Groeseneken: imec, Leuven, Belgium; ESAT, KU Leuven, Leuven, Belgium

We report TCAD simulation studies on nanowire (NW), nanosheet (NS) and forksheet (FS) FET hot-carrier reliability. The simulations entail i) solving the Boltzmann transport equation to obtain the distribution of carriers over energy in the devices, ii) calculation of interface state generation at the channel/gate stack interface and charging of bulk defects in dielectrics, and iii) evaluation of how the generated/trapped charges affect the FET I-V. We discuss the models used in state-of-the-art hot-carrier simulation flows, anneal measurements to probe hot-carrier induced interface defects, the validity of the simulation models in the (V_g, V_d) bias space by comparing simulations to NW FET measurements and the conclusions the hot-carrier simulations provide for NS and FS FETs.

11:05 a.m.
2A.2 - Towards a Universal Model of Dielectric Breakdown, Andrea Padovani: Engineering Department "Enzo Ferrari" (DIEF), University of Modena and Reggio Emilia, Via P. Vivarelli 10, 41125 Modena (MO), Italy, Paolo La Torraca: Department of Sciences and Methods for Engineering (DISMI), University of Modena and Reggio Emilia, Via G. Amendola 2, 42122 Reggio Emilia (RE), Italy, Jack Strand: Department of Physics and Astronomy, University of College London, Gower Street, London WC1E 6BT, UK; Applied Materials-MDLx Italy, Reggio Emilia, and with Nanolayers Research Computing Ltd., London, UK, Alexander Shluger: Department of Physics

and Astronomy, University of College London, Gower Street, London WC1E 6BT, UK, Valerio Milo, Luca Larcher: MDLx Italy, Applied Materials, Via Meuccio Ruini 74/L, 42124 Reggio Emilia (RE), Italy

We present a microscopic breakdown (BD) model in which chemical bonds are weakened by carrier injection and trapping into pre-existing structural defects (precursors) and by the electric field. The model goes much beyond the existing ones by consistently explaining the role of both current (a weakness of the E model) and temperature (a weakness of the power-law model), along with the role of the electric field. It also explains the non-Arrhenius temperature dependence of BD. It suggests a new comprehensive physics-based framework (with tight connections to material properties) reconciling the many breakdown theories proposed so far (E, power-law, 1/E, …) within a more universal breakdown model.

11:30 a.m.

2A.3 - Analysis of TDDB Lifetime Projection in Low Thermal Budget HfO$_2$/SiO$_2$ Stacks for Sequential 3D Integrations, Andrea Vici; KU Leuven, 3001 Leuven, Belgium; Imec, 3001 Leuven, Belgium, R. Degraeve, P. J. Roussel, J. Franco, B. Kaczer: Imec, 3001 Leuven, Belgium, I. De Wolf: KU Leuven, 3001 Leuven, Belgium; Imec, 3001 Leuven, Belgium

We study the impact of fabrication thermal budget on stress-induced defect generation in HfO$_2$/SiO$_2$ stacks compatible with novel Sequential 3D integration. By using stress-induced leakage current (SILC) spectroscopy we show that gate stacks fabricated at low thermal budget, compatible with top-tier integration have a significant pre-existing defect density. We use breakdown and successive breakdown statistics to estimate the number of percolation paths at time zero as a function of the area. Finally, we introduce a modified all-in-one reliability plot that incorporates the impact of the pre-existing defect density on lifetime projection.

11:55 a.m.
2A.4 - Signal duration Sensitive Degradation in Scaled Devices, G. Bersuker: M2D Solutions, Austin, TX, USA, E. Tang, D. Veksler: MTD, The Aerospace Corporation Los Angeles, CA, USA

Defect generation controlling device degradation is found to be highly sensitive to the signal duration in circuitry-relevant operation frequencies (GHz). Stressing devices in ns- time range reveals greatly extended device lifetimes compared to conventional evaluation conditions. The role of energy generation/dissipation in scaled devices is discussed.

2B – NC (Neuromorphic Computing Reliability)
Tuesday, March 28, 10:35 a.m. – 12:20 p.m. PDT
Venue: Regency I-II-III

10:40 a.m.
2B.1 - Impact of Phase-Change Memory Drift on Energy Efficiency and Accuracy of Analog Compute-in-Memory Deep Learning Inference (Invited), Martin M. Frank, Ning Li, Malte J. Rasch, Shubham Jain, Ching-Tzu Chen, Ramachandran Muralidhar, Jin-Ping Han, Vijay Narayanan: IBM T. J. Watson Research Center Yorktown Heights, NY, USA, Timothy M. Philip, Kevin Brew, Andrew Simon, Iqbal Saraf, Nicole Saulnier: IBM Research - Albany Albany, NY, USA, Irem Boybat, Stanislaw Wołniak, Abu Sebastian: IBM Research - Zurich Rüschlikon, Switzerland, Pritish Narayanan, Charles Mackin, An Chen, Hsinyu Tsai, Geoffrey W. Burr: IBM Research - Almaden San Jose, CA, USA

Among the emerging approaches for deep learning acceleration, compute-in-memory (CIM) in crossbar arrays, in conjunction with optimized digital computation and communication, is attractive for achieving high execution speeds and energy efficiency. Analog phase-change memory (PCM) is particularly promising for this purpose. However, resistance typically drifts, which can degrade deep learning accuracy over time. Herein, we first discuss

drift and noise mitigation by integrating projection liners into analog mushroom-type PCM devices, as well as tradeoffs with dynamic range. We then study their impact on inference accuracy for the Transformer-based language model BERT. We find that accuracy loss after extended drift can be minimal with an optimized mapping of weights to cells comprising two pairs of liner PCM devices of varying significance. Finally, we address the impact of drift on energy consumption during inference through a combination of drift, circuit, and architecture simulations. For a range of typical drift coefficients, we show that the peak vector-matrix multiplication (VMM) energy efficiency of a recently proposed heterogeneous CIM accelerator in 14 nm technology can increase by 3% to 15% over the course of one day to ten years. For convolutional neural network (CNN), long short-term memory (LSTM) and Transformer benchmarks, the increase in sustained energy efficiency remains below 10%, being greatest for models dominated by analog computation. Longer VMM integration times increase the energy impact of drift.

11:05 a.m.
2B.2 - ReRAM CiM Fluctuation Pattern Classification by CNN Trained on Artificially Created Dataset, Ayumu Yamada, Naoko Misawa, Chihiro Matsui, Ken Takeuchi: Dept. of Electrical Engineering and Information Systems, The University of Tokyo Tokyo, Japan

A CNN-based Fluctuation Pattern Classifier (FPC) is proposed. FPC is fully trained on the artificially created dataset with assumed fluctuation patterns such as random telegraph noise (RTN) and Oxygen Vacancy movement. FPC is applied to the measured ReRAM signals under different write conditions before read cycles and physical models are established based on the classification results. Proposed fluctuation reduction write (FRW) reduces ReRAM fluctuation rate by 35.1% to improve the inference accuracy of neural network.

11:30 a.m.
2B.3 - Neuromorphic Computation-in-Memory System (Invited), Ken Takeuchi; Department of Electrical Engineering and Information Systems Institution, The University of Tokyo, Tokyo, Japan

For edge AI applications, this paper overviews neuromorphic computing with CiM, Computation-in-Memory with non-volatile memories. AI accelerators like CiM will be heterogeneously integrated with traditional processors such as CPUs. To extremely suppress energy of edge AI, the heterogeneous integration of sensors like event-based sensors and CiM is promising. Approximate Computing for a wide range of fields such as system-level, circuit-level and device-level resolves the memory trade-off. By tolerating some degree of device errors, the performance, energy and cost of CiM are improved. This paper covers neural networks such as Convolutional Neural Network (CNN), Recurrent Neural Network (RNN) as well as event driven Spiking Neural Network (SNN) and Reservoir Computing.

11:55 a.m.
2B.4 - Thermal Induced Retention Degradation of RRAM-Based Neuromorphic Computing Chips, Awang Ma, Bin Gao, Xing Mou, Peng Yao, Yiwei Du, Jianshi Tang, He Qian, Huaqiang Wu: School of Integrated Circuits, BNRist, Tsinghua University, Beijing 100084, China

The retention characteristic of RRAM devices will obviously decrease the computing reliability of RRAM-based neuromorphic computing chips. In this paper, with the help of thermal simulation, we evaluated the thermal effect on the retention characteristic of RRAM devices and the computing accuracy of RRAM-based neuromorphic computing chips. We find weight dual allocation can achieve < 1% accuracy loss in ten years, as compared to 1% accuracy loss in just 4.6 days when one 1T1R unit is used to express one weight. The results also show that the lower temperature can also help to improve the computing reliability of neuromorphic computing chips.

2C – GaN (GaN Power Device)
Tuesday, March 28, 10:35 a.m. – 12:20 p.m. PDT
Venue: Regency IV-V-VI

10:40 a.m.

2C.1 - Reliability Issues of Gate Oxides and p-n Junctions for Vertical GaN Metal-Oxide-Semiconductor Field-Effect Transistors (Invited), Tetsuo Narita, Daigo Kikuta, Kenji Ito, Tomoyuki Shoji, Tomohiko Mori, Satoshi Yamaguchi, Yasuji Kimoto: Toyota Central R&D Labs., Inc., Nagakute, Aichi 480-1192, Japan, Kazuyoshi Tomita, Masakazu Kanechika, Takeshi Kondo, Tsutomu Uesugi, Jun Kojima, Jun Suda: Institute of Materials and Systems for Sustainability (IMaSS), Nagoya University, Nagoya 464-8601, Japan, Yoshitaka Nagasato, Satoshi Ikeda: MIRISE Technologies Corporation, Nisshin, Aichi 470-0111, Japan, Hiroki Watanabe: DENSO CORPORATION, Nisshin, Aichi 470-0111, Japan, Masayoshi Kosaki, Tohru Oka: TOYODA GOSEI Co., Ltd Ama, Aichi 490-1207, Japan

We focus on reliability issues of gate oxides and p-n junctions to realize vertical GaN metal-oxide-semiconductor field-effect transistors (MOSFETs). An annealed AlSiO gate oxide on GaN displayed a lifetime of over 20 years at 150 °C and suppressed positive bias instability in MOSFETs. The key to high channel mobility and stability under positive gate bias is the interface structure designed to minimize oxide border traps. We also evaluated the reliability of GaN p-n diodes (PNDs) on freestanding GaN substrates with different threading dislocation densities. The reverse leakage for PNDs involving threading dislocations was explained by variable-range hopping, while the reverse leakage for dislocation-free PNDs was dominated by band-to-band tunneling. The fabricated PNDs demonstrated excellent robustness under high-temperature reverse bias. However, after continuous forward current stress, reverse leakage pathways were formed at threading screw dislocations, which should be minimized in future GaN substrates.

11:05 a.m.

2C.2 - A Common Hard-Failure Mechanism in GaN HEMTs in Accelerated Switching and Single-Pulse Short-Circuit Tests, D. Wieland: Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria; TU Wien, Gusshausstraße 25, 1040, Vienna, Austria, S. Ofner: Kompetenzzentrum Automobil- und Industrieelektronik (KAI), Europastraße 8, 9524 Villach, Austria, M. Stabentheiner: Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria; TU Wien, Gusshausstraße 25, 1040, Vienna, Austria, B. Butej: Kompetenzzentrum Automobil- und Industrieelektronik (KAI), Europastraße 8, 9524 Villach, Austria; TU Wien, Gusshausstraße 25, 1040, Vienna, Austria, C. Koller: Kompetenzzentrum Automobil- und Industrieelektronik (KAI), Europastraße 8, 9524 Villach, Austria, J. Sun: Infineon Technologies Americas Corp, El Segundo, CA 90245, United States of America, A. Minetto: Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria, K. Reiser: Infineon Technologies Germany AG, am Campeon 1-15, 85579 Neubiberg, Germany, O. Häberlen: Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria, M. Nelhiebel: Kompetenzzentrum Automobil- und Industrieelektronik (KAI), Europastraße 8, 9524 Villach, Austria, M. Glavanovics: Kompetenzzentrum Automobil- und Industrieelektronik (KAI), Europastraße 8, 9524 Villach, Austria, D. Pogany: TU Wien, Gusshausstraße 25, 1040, Vienna, Austria, C. Ostermaier: Infineon Technologies Austria AG, Siemensstraße 2, 9500 Villach, Austria

We report that the hard-failure mechanism observed in single-pulse short-circuit (SPSC) stress tests can also be observed in repetitive hard-switching stress tests as Dynamic High Temperature Operating Lifetime (D-HTOL) and Switching Accelerated Life Test (SALT). This is independent of the device and technology concept in lateral power GaN HEMTs. Thus, the failure physics of two different failure modes can be related to a common model. Our findings enable a better understanding of the different primary and secondary degradation modes and their implication on application lifetime models of different GaN technology concepts.

11:30 a.m.

2C.3 - High-Temperature PBTI in Trench-Gate Vertical GaN Power MOSFETs: Role of Border and Semiconductor Traps, D. Favero, A. Cavaliere, C. De Santi: Department of Information Engineering, University of Padova, via Gradenigo 6/b, 35131, Padova, Italy, M. Borga: Imec, Kapeldreef 75, 3001, Leuven, Belgium, W. Gonçalez Filho: CMST, imec and Ghent University, Technologiepark 126, Ghent 9052, Belgium, K. Geens: Imec, Kapeldreef 75, 3001, Leuven, Belgium, B. Bakeroot: CMST, imec and Ghent University, Technologiepark 126,

Ghent 9052, Belgium, S. Decoutere: Imec, Kapeldreef 75, 3001, Leuven, Belgium, G. Meneghesso: Department of Information Engineering, University of Padova, via Gradenigo 6/b, 35131, Padova, Italy, E. Zanoni: Department of Information Engineering, University of Padova, via Gradenigo 6/b, 35131, Padova, Italy, M. Meneghini: Department of Information Engineering, University of Padova, via Gradenigo 6/b, 35131, Padova, Italy; Department of Physics and Astronomy, University of Padova, via Marzolo 8, 35151, Padova, Italy

For the first time we investigate the positive threshold voltage instability in GaN-based trench gate MOSFETs in the high-temperature regime (150-240 °C). First, by inverse Laplace transform we determine the equivalent distribution of activation energies of the traps responsible for PBTI, with a peak at 0.75 eV from the conduction band of GaN. Second, we demonstrate that the recovery transients have a non-monotonic trend. This result, never described before, is attributed to the interplay between electron de-trapping from border traps, and hole de-trapping from defects in the p-type body layer, located 0.65 eV above the valence band energy of GaN, and preliminary ascribed to gallium vacancies in the semiconductor. Results provide relevant insight for optimizing the high-temperature stability of GaN vertical FETs.

11:55 a.m.
2C.4 - Trapping in Al2O3/GaN MOScaps Investigated by Fast Capacitive Techniques, Manuel Fregolent, Alberto Marcuzzi, Carlo De Santi: Department of Information Engineering, University of Padova, Via Giovanni Gradenigo 6B, 35131 Padova, Italy; IUNET - National Interuniversity Consortium for Nanoelectronics, Italy, Eldad Bahat Treidel: Ferdinand-Braun-Institut (FBH), 12489 Berlin, Germany, Gaudenzio Meneghesso, Enrico Zanoni: Department of Information Engineering, University of Padova, Via Giovanni Gradenigo 6B, 35131 Padova, Italy; IUNET - National Interuniversity Consortium for Nanoelectronics, Italy, Matteo Meneghini: Department of Information Engineering, University of Padova, Via Giovanni Gradenigo 6B, 35131 Padova, Italy; IUNET - National Interuniversity Consortium for Nanoelectronics, Italy; Department of Physics and Astronomy, University of Padova, via Marzolo 8, 35131 Padova, Italy

We present a detailed investigation of charge trapping processes in Al_2O_3/GaN vertical MOS capacitors, detected by means of advanced capacitance measurements. The devices stressed at positive bias present a trapping mechanism that results in an increase of the flatband voltage, while under negative voltages the negative charge stored in bulk and interface states is released with a leftward shift of the C-V characteristic. We also demonstrated that the formation of the hump in depletion regime is the result of trapping of electrons at the oxide-semiconductor interface. The detected behavior is modeled by considering the DIT profile extrapolated by photoassisted CV measurements. The results provide relevant input for the design of stable and reliable MOS transistors based on GaN.

Break
Tuesday, March 28, 12:00 p.m. – 01:30 p.m. PDT

3A – MR (Memory Reliability)
Tuesday, March 28, 01:25 p.m. – 03:35 p.m. PDT
Venue: Regency Main

01:30 p.m.
3A.1 - Write-Error-Rate of Spin-Transfer-Torque MRAM (Invited), Daniel C. Worledge: IBM Almadén Research Center, IBM Research, San Jose, USA

Embedded Spin-Transfer Torque Magnetoresistive Random Access Memory (STT-MRAM) is now a standard foundry offering for embedded non-volatile memory applications at the 28 nm node and below, where it replaces embedded Flash, due to lower development costs. The switch from in-plane to perpendicularly magnetized magnetic materials enabled reliable operation and a scaling path. Write-error-rate is the key reliability challenge for STT-

MRAM While due to fundamental physics, write-error-rate of STT-MRAM can be engineered to meet even aggressive product specifications.

01:55 p.m.
3A.2 - Double-Sided Row Hammer Effect in Sub-20 nm DRAM: Physical Mechanism, Key Features and Mitigation, Longda Zhou, Jie Li, Zheng Qiao, Pengpeng Ren: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong university and Peking University, China; Department of Micro/Nano Electronics, SEIEE, Shanghai Jiao Tong University, Shanghai 200240, China, Zixuan Sun: School of Integrated Circuit, Peking University, Beijing 100871, China, Jianping Wang, Blacksmith Wu: ChangXin Memory Technologies, Hefei 230601, China, Zhigang Ji: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong university and Peking University, China; Department of Micro/Nano Electronics, SEIEE, Shanghai Jiao Tong University; Beijing Superstring Academy of Memory Technology, Beijing, 100176, China, Runsheng Wang: School of Integrated Circuit, Peking University, Beijing 100871, China; Beijing Superstring Academy of Memory Technology, Beijing, 100176, China, Kanyu Cao: ChangXin Memory Technologies, Hefei 230601, China, Ru Huang: School of Integrated Circuit, Peking University, Beijing 100871, China

The double-sided row hammer (rh) effect at the silicon level for sub-20 nm dynamic random access memory (DRAM) is systematically investigated for the first time. Based on 3D TCAD simulation, the impacts of capacitive crosstalk and electron migration are investigated. The latter with trap assistance is found the dominant mechanism behind the enhancement of 1 failure and the alleviation of 0 failure for double-sided rh. Moreover, rh dependences on data pattern, timing parameters and technology nodes are compared under different rh conditions. A trade-off of retention time (tret) between 1 failure and 0 failure should be considered when suppressing the double-sided rh effect. With the co-optimization of key process parameters, tret for double-sided rh-induced 1 failure can be improved by 220 times.

02:20 p.m.
3A.3 - A New Ramp Stress Reliability Assessment on Pulse Energy Based OTS Switching Operation, P. C. Chang, P. J. Liao, C. H. Wu, Y. C. Chang, D. H. Hou, E. Ambrosi, H. Y. Lee, J. H. Lee, X. Y. Bao: Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan

With the increasing demand of Ovonic Threshold Switching (OTS) endurance performance, reliability acceleration model becomes imperative to speed up lifetime assessment. In this work, we develop a new ramp stress methodology to perform fast measurement with the proof of consistent lifetime and comparable distribution slope with respect to conventional time-consuming endurance tests. We have successfully proved material and polarity dependence of device endurance in GeCTe (GCT) based alloys thanks to this new method. This has been proved to largely reduce reliability evaluation time and provide a real time die-level reliability acceleration model for endurance prediction.

02:45 p.m.
3A.4 - Comprehensive Analysis of Hole-Trapping in SiN Films with a Wide Range of Time Constants Based on Dynamic C-V, Harumi Seki, Reika Ichihara, Yusuke Higashi, Yasushi Nakasaki, Masumi Saitoh, Masamichi Suzuki: Institute of Memory Technology, R&D Kioxia Corporation, Yokohama, Japan

The charge trapping characteristics in the silicon nitride (SiN) film were comprehensively studied by using dynamic CV technique with charge centroid analysis under various temperatures. We found two types of hole traps with short (long) time constant which capture holes at low (high) electric field. Traps with time constant down to 10 µs can be detected thanks to dynamic CV. For each kind of traps, the trapped charge density, spatial position, and the activation energy of de-trapping process are clarified, which are essential to understand the reliability issues of charge-trap memory devices.

3B – SiC (Wide-Bandgap Semiconductors-SiC)
Tuesday, March 28, 01:25 p.m. – 03:35 p.m. PDT
Venue: Regency I-II-III

01:30 p.m.
3B.1 - Towards Understanding the Physics of Gate Switching Instability in Silicon Carbide MOSFETs, Katja

Waschneck: Infineon Technologies AG, 85579 Neubiberg, Germany, Hans Reisinger: Infineon Technologies AG, 85579 Neubiberg, Germany, Judith Berens: Infineon Technologies Austria AG, 9500 Villach, Austria, Thomas Aichinger: Infineon Technologies Austria AG, 9500 Villach, Austria, Paul Salmen: Infineon Technologies AG, 85579 Neubiberg, Germany, Gerald Rescher: Infineon Technologies Austria AG, 9500 Villach, Austria, Wolfgang Gusting: Infineon Technologies AG, 85579 Neubiberg, Germany, Tibor Grasser: Institute for Microelectronics, Technische Universität Wien, 1040 Wien, Austria

Bias temperature instability (BTI) is a well-investigated degradation mechanism in technologies based on silicon, gallium nitride, or silicon carbide (SiC). Essentially, it leads to a drift in the threshold voltage and to a reduction in mobility after application of a gate bias, and becomes worse at elevated temperatures. However, as discovered recently, the threshold voltage drift of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) has different properties than those known from BTI when the gate terminal of the device is switched in a bipolar mode. This new degradation mechanism has recently been termed gate switching instability (GSI). To further understand this degradation mechanism and the underlying physics, we have used pre- and post-stress impedance characterization and in-situ ultra-fast threshold voltage measurements. Most importantly, we show that the gate switching leads to the creation of fast, acceptor-like interface defects that lead to a shift in threshold voltage, and hence appear to be responsible for GSI.

01:55 p.m.
3B.2 - Extended Analysis of Power Cycling Behavior of TO-Packaged SiC Power MOSFETs, Ivana

Kovacevic-Badstuebner, Salvatore Race, Ulrike Grossner: Advanced Power Semiconductor Laboratory (APS), ETH Zurich, 8092 Zurich, Switzerland, Elena Mengotti, Christoph Kenel, Enea Bianda: ABB Switzerland Ltd., Corporate Research Center 5405 Baden, Switzerland, Joni Jormanainen: ABB Drives Oy, 00380 Helsinki, Finland

This paper presents an extended analysis of TO-packaged SiC power MOSFETs after power cycling (PC) tests. Namely, it is shown that initially present voids in soft lead-based solder die attach disappear not only after certain number of active PC tests, but also after thermal shock tests. Hereby, the conclusion that solder die attach is not the weak spot of SiC power MOSFET packages with an epoxy mold compound (EMC) encapsulation is further supported. Furthermore, an electro-thermo-mechanical (ETM) model developed in-house is used to correlate the dominant wear-out failure of bond wires to the PC test parameters such as heating current, temperature amplitude, and heating on-time, as well as to the thickness of top source die metallization.

02:20 p.m.
3B.3 - V-Ramp Test and Gate Oxide Screening under the "lucky" Defect Model, Kin P. Cheung: National

Institute of Standards & Technology, Gaithersburg, MD 20899 USA

The persistent (after exhaustive wafer cleaning) extrinsic breakdown distribution of thick gate oxides requires an early breakdown mechanism that goes beyond the popular local thinning model to explain. The success of the 'Lucky' defect model in fulfilling this role deserves a further exploration of its implications. This work examines the implications of using the V-Ramp and the high-voltage screening methods to identify early failures. In this study, it is shown that the V-Ramp method fails to produce useful information about the oxide quality at operation voltages and that the high-field screening method fails to screen out early failures.

02:45 p.m.
3B.4 - Investigation of Different Screening Methods on Threshold Voltage and Gate Oxide Lifetime of SiC Power MOSFETs, Limeng Shi, Shengnan Zhu, Jiashu Qian, Michael Jin: Dept. of Electrical & Computer Engineering, The Ohio State University, Columbus, Ohio, USA, Monikuntala Bhattacharya, Marvin H. White, Anant K. Agarwal: Dept. of Electrical & Computer Engineering, The Ohio State University, Columbus, Ohio, USA, Atsushi Shimbori, Tianshi Liu: Ford Motor Company, Dearborn, Michigan, USA

The effects of different screening methods for non-infant extrinsic defects on the gate oxide reliability of commercial 1.2 kV 4H-SiC power MOSFETs are investigated. This study aims to find the optimal screening voltage and duration for high gate-voltage pulse screening and long-term burn-in with acceptable constraints on threshold voltage (V_{th}) shift and oxide lifetime degradation. The V_{th} is monitored during the stress and recovery process under various screening conditions. SiC MOSFETs with the trench structure can be screened at high voltages due to the thicker gate oxide. Moreover, an optimized screening method is proposed which uses a multi-pulse mode screening technique to reduce the effects of high gate voltages on the permanent shift of V_{th}. Furthermore, constant-voltage time-dependent dielectric breakdown measurements are conducted on SiC MOSFETs with and without high-voltage screening. The results reveal that high voltage applied for a short period of time (≤ 1 s) has no obvious negative impact on the oxide lifetimes of SiC MOSFETs.

3C – PK (Packaging and 2.5/3D Assembly)
Tuesday, March 28, 01:25 p.m. – 03:35 p.m. PDT
Venue: Regency IV-V-VI

01:30 p.m.
3C.1 - Transient Leakage Current as a Non-Destructive Probe of Wire-Bond Electrochemical Failures, M. Asaduz Zaman Mamun: Purdue University, West Lafayette, IN 47907, USA, Amar Mavinkurve, Michiel van Soestbergen: NXP Semiconductors, Nijmegen, the Netherlands, Muhammad A. Alam: Purdue University, West Lafayette, IN 47907, USA

The electrochemical failures observed in the accelerated stress test (e.g., HAST/ THB) are correlated to the sequential processes of spatial and transient ionic distribution in the Epoxy Molding compound (EMC)/underfill materials, redox reaction, and the formation of Intermetallic Compounds (IMCs). Unfortunately, HAST tests require fully assembled IC, and can only occur relatively late in the process development. Here, we provide a new prediction approach to quantify bondpad/EMC interfacial charge dynamics using thermally stimulated charging current (TSCC). TSCC also probes EMC ionic transport mechanisms. We assess the universal (dispersive) nature of ionic transport in the EMC using measured and simulated TSCC for industry-grade EMC samples with high halide concentrations (13–200 ppm). Finally, our proposed ion-assisted corrosion failure model, along with the predicted TSCC, elucidates the impact of halide concentration on bond wire electrochemical failures and may be used as a non-destructive method for predicting electrochemical failures of ICs. Most importantly, our approach may serve as an early indicator of the corrosion challenges long before the packaged IC has actually been fabricated.

01:55 p.m.
3C.2 - Wafer Level Chip Scale Package Failure Mode Prediction using Finite Element Modeling, Viktor Dudash: GlobalFoundries Dresden Module One LLC & Co. KG, Dresden, Germany; Institute of Electronic Packaging Technology TU Dresden Dresden, Germany, Kashi Vishwanath Machani, Bjoern Boehme, Simone Capecchi: GlobalFoundries Dresden Module One LLC & Co. KG, Dresden, Germany, Jungtae Ok: GlobalFoundries Singapore Pte. Ltd.-Korea Seoul, South Korea, Karsten Meier: Institute of Electronic Packaging Technology TU Dresden Dresden, Germany, Frank Kuechenmeister, Marcel Wieland: GlobalFoundries Dresden Module One LLC & Co. KG, Dresden, Germany, Karlheinz Bock: Institute of Electronic Packaging Technology TU Dresden Dresden, Germany

In this study a Finite Element Model (FEM) was designed in order to predict the reliability behavior of 7×7 mm^2 Wafer Level Chip Scale Packages (WLCSP) during board level thermal cycling tests, considering different solder material models for SAC405 and SACQ interconnects. A significant difference in plastic strains within the package was observed for a variety of solder material models: Compared to SACQ interconnects an approximate 70% plastic strain increase in solder and a 35% plastic strain reduction in the polyimide passivation layer was observed for packages with SAC405 interconnects. Simulations were verified by experimental thermal cycling test data done at board level. During thermal cycling, packages showed different failure modes depending on the interconnect material used in the package. Also, SAC405 showed earlier failure. Maximum strain obtained from simulations was used as an indicator of potential failure locations for the solder alloy and polyimide layer. The proposed model setup enables precise simulation results, which are well aligned with the actual experimental findings on the behavior of WLCSP with SAC405 and SACQ interconnects.

02:20 p.m.
3C.3 - Knowledge Based Qualification for Thermal Interface Material Reliability, E. Armagan, A. Saha: Assembly Test Technology Development Quality and Reliability, Intel Corporation, Chandler, Arizona, U.S.A, K. C. Liu, B. Gebrehiwot, M. Cartas, A. Das, T. Rawlings, P. Raghavan: Assembly Test Technology Development Core Competency, Intel Corporation, Chandler, Arizona, U.S.A,

For thermo-mechanical reliability, the difference between the actual use stress and accelerated qualification stress is most apparent in temperature cycling stress due to isothermal large temperature delta applied during temperature cycling vs. non-uniform low amplitude thermal changes in use condition. Power cycling is alternatively utilized to characterize these differences with common industry practice for power cycling is to stress functional devices since it requires to power on and off the components. To overcome the limited failure information that can be learned through functional device stressing, a novel power cycling tool is designed to stress test vehicles with dedicated electrical/thermal structures enabling targeted uniform or nonuniform power to be applied during stress and resulting temperature delta can be accurately measured through dedicated temperature sensors in the chip and package. Data collected with this tool is then compared with calculated acceleration through temperature cycling stress. Comparison shows temperature cycling based life estimations are conservative for thermal interface material degradation estimations. This work also encompassed use condition data collection and finite element modeling to derive the final knowledge-based requirements.

02:45 p.m.
3C.4 - Recent Advances on Electromigration in Cu/SiO2 to Cu/SiO2 Hybrid Bonds for 3D Integrated Circuits, S. Moreau, D. Bouchu: CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France, J. Jourdon: STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France, B. Ayoub: CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France; STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France; IMS Laboratory, University of Bordeaux, UMR 5218, F-33405 Talence, France, S. Lhostis, H. Frémont, P. Lamontagne: STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France

With hybrid bonding (HB) pitch reduction, many challenges are arising. One of them is related to the reliability of HB-based interconnects and in particular their electromigration performances as electromigration (EM)-related degradation is intimately linked to the electrical current in addition to temperature and mechanical stresses. This study highlights a change in the failure modes for EM-related failures in HB-based interconnects when decreasing the interconnect pitch from 6.84 down to 1.44 μm. The weakest link moves from the BEOL levels to hybrid bonding ones but without affecting the projected performance under use conditions. Additional studies done on design aspects do not evidence any negative impact on the electromigration resistance of the HB brick.

Break
Tuesday, March 28, 03:25 p.m. – 03:45 p.m. PDT

4A – EM (Emerging Memory)
Tuesday, March 28, 03:50 p.m. – 05:35 p.m. PDT
Venue: Regency Main

03:55 p.m.
4A.1 - Material Instabilities in the TaOx-Based Resistive Switching Devices, M. Skowronski: Dept. Materials Science and Engineering, Carnegie Mellon University, Pittsburgh, PA 15213, USA

Oxide-based resistive switching devices offer an attractive set of characteristics for embedded memories and neuromorphic computing. However, their endurance is limited with the origin of failure mechanisms not firmly established. Transmission electron microscopy results on TiN/TaO$_x$/TiN structures suggest that the primary reason is the intrinsic instability of TaO$_x$ in the middle of the composition range. This material separates into Ta- and O-rich phases that affect the filament morphology and can result in either stuck-in-high or stuck-in-low resistance state failure. An additional factor affecting endurance of switching devices is the interdiffusion at the electrode-functional oxide interfaces.

04:20 p.m.
4A.2 - Investigation of Resistance Fluctuations in ReRAM: Physical Origin, Temporal Dependence and Impact on Memory Reliability, L. Reganaz: CEA, LETI, MINATEC Campus, 38000, Grenoble, France; Université Grenoble Alpes, 38000, Grenoble, France, D. Deleruyelle: INL CNRS, INSA Lyon, 69621, Lyon, France, Q. Rafhay: Université Grenoble Alpes, Université Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC, 38000, Grenoble, France, J. Minguet Lopez, N. Castellani, J. F. Nodin: CEA, LETI, MINATEC Campus, 38000, Grenoble, France, A. Bricalli, G. Piccolboni, G. Molas: Weebit Nano Ltd, F. Andrieu: CEA, LETI, MINATEC Campus, 38000, Grenoble, France

We investigate the impact of ReRAM resistance fluctuations in a 16kb memory array. ReRAM retention and read current fluctuations are the main factors limiting the reliability of the array. A KMC-based 3D simulation framework is introduced for a complete physical description of the observed mechanisms. After individual cell relaxation (up to one second at room temperature) and resistance distribution stabilization, single cell level fluctuations still occur, especially in HRS. Oxygen vacancy migration and recombination, RTN and 1/f noise components contribute to the dynamic evolution. In a first phase, higher and faster current fluctuations are measured due to RTN and Vo low energy migration (1-10min at 25°C). In a second phase, the contribution of Vo migration tends to decrease as they neutralize in clusters or diffuse (>10min at 25°C). Finally, the impact of individual cell fluctuations on the variability and reliability of memory array is analyzed.

04:45 p.m.
4A.3 - Unveiling Retention Physical Mechanism of Ge-Rich GST ePCM Technology, Luca Laurin: Smartpower T&RD, STMicroelectronics, Via Olivetti 2, 20864 Agrate Brianza, Italy, M. Baldo: Smartpower T&RD, STMicroelectronics, Via Olivetti 2, 20864 Agrate Brianza, Italy; Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IUNET, p.za Leonardo da Vinci 32, 20133, Milano, Italy, E. Petroni, G. Samanni, L. Turconi, A. Motta, M. Borghi: Smartpower T&RD, STMicroelectronics, Via Olivetti 2, 20864 Agrate Brianza, Italy, A. Serafini, D. Codegoni: FMT Physical Lab, STMicroelectronics, Via Olivetti 2, 20864 Agrate Brianza, Italy, M. Scuderi: CNR-IMM, Catania, Strada VIII n.5 Zona Industriale, Catania 95121, Italy, S. Ran, A. Claverie: CEMES-CNRS and Universite de Toulouse 29 Rue Jeanne Marvig, 31055, Toulouse, France, D. Ielmini: Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IUNET, p.za Leonardo da Vinci 32, 20133, Milano, Italy, R. Annunziata, A. Redaelli: Smartpower T&RD, STMicroelectronics, Via Olivetti 2, 20864 Agrate Brianza, Italy

In this work, a comprehensive study of Ge-rich Phase Change Memory set and reset state retention realized by coupling electrical and physical characterizations is presented. The presence of amorphous residuals inside the active region of PCM devices is, for the first time, demonstrated through High Resolution Scanning Transmission Electron Microscopy. The role of such formations was studied by means of electrical characterization and supported by modeling analysis. By comparing the low and high state resistive behavior the retention physics has been analytically modeled with the same framework for both states.

4B – CR (Circuit Reliability and Aging)
Tuesday, March 28, 03:50 p.m. – 05:35 p.m. PDT
Venue: Regency I-II-III

03:55 p.m.
4B.1 - Challenges and Solutions to the Defect-Centric Modeling and Circuit Simulation of Time-Dependent Variability, Javier Martin-Martinez: Department of Electronic Engineering, Universitat Autonoma Barcelona, 08193 Bellaterra, Spain, Javier Diaz-Fortuny: Department of Electronic Engineering, Universitat Autonoma Barcelona, 08193 Bellaterra, Spain; imec, Kapeldreef 75, 3001 Leuven, Belgium, Pablo Saraza-Canflanca: Instituto de Microelectrónica de Sevilla, (Universidad de Sevilla and CSIC), 41092 Seville, Spain; imec, Kapeldreef 75, 3001 Leuven, Belgium, Rosana Rodriguez: Department of Electronic Engineering, Universitat Autonoma Barcelona, 08193 Bellaterra, Spain, Rafael Castro-Lopez, Elisenda Roca, Francisco V. Fernandez: Instituto de Microelectrónica de Sevilla, (Universidad de Sevilla and CSIC), 41092 Seville, Spain, Montserrat Nafria: Department of Electronic Engineering, Universitat Autonoma Barcelona, 08193 Bellaterra, Spain

Time-Dependent Variability (TDV) phenomena represent a serious concern for device and circuit reliability. To address the TDV impact at circuit level, Reliability-Aware Design (RAD) tools can be used by circuit designers to achieve more reliable circuits. However, this is not a straightforward task, since the development of RAD tools comprises several steps such as the characterization, modeling and simulation of TDV phenomena. Furthermore, in deeply-scaled CMOS technologies, TDV reveals a stochastic nature that can complicate those steps. In this invited paper, we review some of the main challenges that appear in each step of the flow towards the development of RAD tools, providing our solutions to them.

04:20 p.m.
4B.2 - A Unified Aging Model Framework Capturing Device to Circuit Degradation for Advance Technology Nodes, S. Mukhopadhyay: Logic Technology Development Quality and Reliability, Intel Corporation, USA, C. Chen: Quality & Reliability Test Chip Design and Data, Intel Corporation, USA, M. Jamil: Logic Technology Development Quality and Reliability, Intel Corporation, USA, J. Standfest: Quality & Reliability Test Chip Design and Data, Intel Corporation, USA, I. Meric: Logic Technology Development Quality and Reliability, Intel Corporation, USA, B. Gill: Quality & Reliability Test Chip Design and Data, Intel Corporation, USA, S. Ramey: Logic Technology Development Quality and Reliability, Intel Corporation, USA

Transistor aging under complex input waveform stress has been a key concern for device and circuit reliability. The overall Design Technology Co-Optimization (DTCO) is strongly guided by the reliability risk of a single transistor as well as by the reliability performance of the overall IP/product. Although the IP/Product reliability evaluation is most beneficial at the early stages of the technology development, it is often very expensive, and no certain aging model methodology exists to quantify the risks. In this work, for the first time we demonstrate a unified aging model framework, which not only can predict the traditional DC transistor aging, but also can accurately predict aging in various styles of circuits. Various Ring-Oscillators (RO) under arbitrary stress conditions are used to demonstrate model predictability after long-term stress approaching product use conditions. Such consistent framework helps to guide the process technology development, as well as provides for high-confidence product/IP reliability design assurance.

04:45 p.m.
4B.3 - Improving the Tamper-Aware Odometer Concept by Enhancing Dynamic Stress Operation, Javier Diaz-Fortuny: imec, Kapeldreef 75, 3001 Leuven, Belgium, Dishant Sangani: imec, Kapeldreef 75, 3001 Leuven, Belgium; ESAT, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium, Pablo Saraza-Canflanca, Erik Bury, Robin Degraeve, Ben Kaczer: imec, Kapeldreef 75, 3001 Leuven, Belgium

On-chip degradation monitors have recently gained significant relevance because they can provide real-time estimations of IC reliability by exploiting the fundamental physics of BTI and HCD circuit degradation. Moreover, this type of degradation monitors can be used as a tamper detection mechanism to expose counterfeited chips, as we have demonstrated previously. In this context, common ring-oscillator (RO)-based odometers have shown a predominant BTI component over HCD in dynamic stress. This complicates the effort of combining the different degradation kinetics of monitors stressed solely with BTI and HCD for accurate aging determination and counterfeiting detection capability. In this work, we propose and validate two new RO-based odometers to enhance HCD over BTI degradation by (i) a RO with a high order harmonic trigger circuitry and (ii) a RO with I/O pass gates utilized to perform DC HCD. We also extend the tamper-aware odometer concept to a commercial 16 nm FinFET technology with ROs to further exploit the larger HCD component in FinFET technology. Finally, we present not only accelerated degradation tests but also on-chip circuit annealing by means of dedicated on-chip heaters and off-chip furnace anneal. From our findings, we derive an optimal combination of odometers to accurately account for IC age and for a robust tamper-aware monitors combination.

05:10 p.m.
4B.4 - Integrated Test Circuit for Off-State Dynamic Drain Stress Evaluation, J. Hai, F. Cacho, X. Federspiel, T. Garba-Seybou: STMicroelectronics, 850 rue Jean Monnet, 38926, Crolles, France, A. Divay: CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France, E. Lauga-Larroze, J.-D. Arnould: Univ. Grenoble Alpes, CNRS, Grenoble INP, Institute of Engineering Univ. Grenoble Alpes, TIMA, Grenoble, France

Dynamic off-state stress for RF applications is investigated via integrated test circuits to enable GHz level testing. We have performed characterization of test circuits to ensure the dynamic stress signal waveform integrity, which is verified against model simulation data. We report a x2 gain on time-to-breakdown at 1GHz against DC TDDB off-state stress. Based on extraction of I_{diin} degradation, no frequency effect is observed from DC to 1GHz off-state stress conditions. Modeling of on-state and off-state interactions based on sum of degradations modes is then demonstrated and supported by experimental data.

4C – GD (Gate/MOL Dielectrics)
Tuesday, March 28, 03:50 p.m. – 05:35 p.m. PDT
Venue: Regency IV-V-VI

03:55 p.m.
4C.1 - Reliability Modeling of Middle-Of-Line Interconnect Dielectrics in Advanced Process Nodes, R. Kasim, C. Lin, C. Perini, J. Palmer, N. Gilda, S. Imam, J. R. Weber: Logic Technology Development Quality and Reliability, TCAD, Hillsboro, OR 97124, USA, C. Wallace: Portland Technology Development Intel Corporation, 2501 NE Century Blvd, Hillsboro, OR 97124, USA, J. Hicks: Logic Technology Development Quality and Reliability, TCAD, Hillsboro, OR 97124, USA

This paper discusses the physics and methodology for estimating the Reliability lifetime of MOL (Middle-Of-Line) dielectrics for advanced process nodes. Both intrinsic and defect reliability aspects of MOL dielectrics are investigated for accurate projection of Reliability lifetime on Intel 4 process technology. Methods to deconvolute the impact of process driven variations on intrinsic Time Dependent Dielectric Breakdown (TDDB) are presented. In addition, a new construct for targeting of the MOL process parameters is also proposed to address challenges with technology scaling and to mitigate risk with pattern fidelity driven variations.

04:20 p.m.

4C.2 - Location of Oxide Breakdown Events under Off-State TDDB in 28nm N-MOSFETs Dedicated to RF Applications, Tidjani Garba-Seybou: STMicroelectronics, 850 Rue Jean Monnet, 38920 Crolles, France; ISEN Yncréa Méditerranée, REER-IM2NP UMR CNRS 7334, Maison des technologies, Place G. Pompidou, 83000 Toulon, France, Xavier Federspiel, Frederic Monsieur, Mathieu Sicre, Florian Cacho, Joycelyn Hai, Alain Bravaix: STMicroelectronics, 850 Rue Jean Monnet, 38920 Crolles, France

A detailed analysis of Off-state gate-oxide breakdown (BD) mode and its location under non-uniform electric field is performed in 28nm FDSOI N-MOSFET devices. We show that hard breakdown (HBD) occurs exclusively from the middle of the channel to the drain overlap extension for Off-state TDDB. HBD is characterized under DC stress with different gate-length LG as a function of drain voltage VDS and temperature. We check that the leakage current is the better monitor for TDDB dependence precursor to HBD under Off-mode stress by using the proper modeling and discussing the different possible origin of the higher form factor β value under Off mode stressing.

04:45 p.m.

4C.3 - GHz AC to DC TDDB Modeling with Defect Accumulation Efficiency Model, Xinwei Yu, Chu Yan, Yarn Ding: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China, Yiming Qu: School of Integrated Circuits, East China Normal University, Shanghai 200241, China, Yi Zhao: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China; School of Integrated Circuits, East China Normal University, Shanghai 200241, China

In this work, AC time-dependent dielectric breakdown (TDDB) of SOI MOSFETs was systematically investigated with considerable experimental data using various stress patterns. It is confirmed that both the time to breakdown (TBD) and hardness of post-breakdown could be improved at GHz frequency. Based on frequency dependence of TDDB lifetime, we propose a comprehensive defect accumulation efficiency (ξ) model related to pulse width, helping to predict AC TDDB lifetime. In addition, new failure mechanisms for on-state TDDB are clarified by weakening HCI coupled effect. This study is significant for lifetime estimation of logic devices under dynamic circuit operations.

05:10 p.m.

4C.4 - Semantic Autoencoder for Modeling BEOL and MOL Dielectric Lifetime Distributions, Weiman Yan: Dept. of Electrical and Computer Engineering, University of Illinois Urbana-Champaign, Urbana, Illinois, USA, Ernest Wu: IBM Research Division, Essex Junction, Vermont, USA, Alexander G. Schwing, Elyse Rosenbaum: Dept. of Electrical and Computer Engineering, University of Illinois Urbana-Champaign, Urbana, Illinois, USA

This paper presents a physics-based machine learning framework for modeling a dielectric lifetime distribution in the presence of manufacturing process variations. It uses a semantic autoencoder that provides insight into the dielectric thickness distribution and parameters of the underlying percolation model. Experiments show that the model is applicable to various types of dielectric films and that including time-zero leakage current as an input improves the model performance. The autoencoder may be configured to model intrinsic break-down or to model breakdown resulting from competing failure mechanisms, e.g. intrinsic and extrinsic.

IRPS 2023 WORKSHOPS

Tuesday, 28 March

6:00 -7:30 PM

Workshop Reception

Regency Terrace

7:30-8:30 PM

WS 1 - FEOL / MOL Reliability - Can We Maintain Same Vmax Specs Despite Scaling?

Chaired By: Pei Jean Liao, TSMC

Regency I-II-III

WS 2 - BEOL Reliability - Can We Maintain Same Jmax Specs with New Materials?

Chaired By: Kristof Croes, imec

Regency IV-V-VI

WS 3 - ESD and Latchup - are Today's EDA Tools Sufficient?

Chaired By: Matthew Hogan, Siemens EDA

Windjamer III-IV

WS 4 - DRAM Stacking Reliability Challenges for New SoCs

Chaired By: Jin-Woo Han, Samsung Electronics

Cypress

WS 5 - Failure Analysis and New Techniques for Fault Isolation in Sub-4nm

Chaired By: Daniel Sullivan, EAG

Big Sur

IRDS I - IEEE International Roadmap for Devices and Systems (IRDS)

Chaired By: Paolo Gargini, IEEE IRDS Chairman

Regency Main

8:30-8:45 PM

Break

8:45-9:45 PM

WS 6 - N2 and Beyond, What are the New Reliability Challenges?

Chaired By: Jacopo Franco, imec

Regency I-II-III

WS 7 - Wide Band Gap Future Reliability Challenges in EV

Chaired By: Don Gajewski, Wolfspeed

Regency IV-V-VI

WS 8 - AI Compute Reliability

Chaired By: Fen Chen, GM Cruise

Windjamer III-IV

WS 9 - Knowledge Base Qualification in Consumer Applications

Chaired By: Sundarshan Rangaraj, Amazon

Cypress

WS 10 – Data Center Semiconductor Field Failures Survey

Chaired By: Chundong Liang, AWS

Big Sur

IRDS II - Challenges and Opportunities for Devices and Systems

Chaired By: Paolo Gargini, IEEE IRDS Chairman

Regency Main

Wednesday, March 29

Keynote 3
Wednesday, March 29, 08:00 a.m. – 08:50 a.m. PDT
Venue: Regency Main

08:00 a.m.
KN3 (Keynote) - Reliability Challenges for the Next Decade of High-Performance Computing, Mark Fuselier; AMD

As classic Moore's law has slowed to a crawl, our industry faces many challenges as we drive the continued scaling of High-Performance Compute solutions. Our industry is spearheading innovation across silicon technology, chiplet integrated advanced packages, high bandwidth I/O, and custom heterogenous compute architectures. These advancements bring new and distinct quality, reliability, and physical failure analysis issues that we must tackle. This keynote will call our community to action while it addresses key innovations necessary over the next decade to push the performance scaling required to support the compute bandwidth required to solve our harshest challenges.

Break
Wednesday, March 29, 08:50 a.m. – 09:10 a.m. PDT

5A – EL (ESD and Latchup (IRPS)
Wednesday, March 29, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency Main

09:15 a.m.
5A.1 - Optimization of SCR for High-Speed Digital and RF Applications in 45-nm SOI CMOS Technology, Shudong Huang: Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign 1308 W. Main St., Urbana, IL 61801 USA, Srivatsan Parthasarathy, Yuanzhong Zhou, Jean-Jacques Hajjar: Analog Devices, Inc., Wilmington, MA, USA, Elyse Rosenbaum: Department of Electrical and Computer Engineering University of Illinois at Urbana-Champaign 1308 W. Main St., Urbana, IL 61801 USA

This work presents a low-leakage silicon-controlled-rectifier (SCR) for ESD protection in a 45-nm PDSOI CMOS technology. The newly proposed trigger circuit utilizes a gate-coupled NMOS to provide a low trigger voltage, making the SCR suitable for gate oxide protection. Reverse body bias is used to achieve a low DC leakage current. The anode-cathode spacing of the SCR is optimized to provide a low overshoot voltage while avoiding punchthrough. The optimized SCR shows up to 50% improvement in voltage overshoot during very fast transients on the CDM timescale.

09:40 a.m.
5A.2 - Collector Engineering of ESD PNP in BCD Technologies, Yujie Zhou: Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA, David LaFonteese: Texas Instruments, Dallas, TX 75243 USA, Elyse Rosenbaum: Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA

PNP bipolar transistors are an ESD protection solution for high-voltage analog products. Using both measurements and TCAD simulations, this work analyzes the effects of the deep collector P-Well implants on the I-V characteristic of a high-voltage lateral PNP. Design guidelines for a PNP protection device are formulated; specifically, it is recommended to use a deep and narrow collector and minimize vertical non-uniformity in the doping profile.

10:05 a.m.
5A.3 - Impact of Thin-Oxide Gate on the On-Resistance of HV-PNP under ESD Stress, Monishmurali M.: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India, Nagothu Karmel Kranthi: Texas Instruments Inc, Bangalore, India, Gianluca Boselli: Texas Instruments Inc, Dallas, USA, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India

Physical insights into the impact of the thin-oxide polysilicon gate on the on-resistance of DeMOS-based HV-PNP are developed using detailed TCAD simulation. Turn-on and eventual failure mechanisms in HV-PNP are discussed. The impact of thin-oxide polysilicon placed over the N-Well and P-Well regions is investigated separately. The physics of regenerative bipolar degradation and its effect of dynamic on-resistance is understood as a function of thin-oxide placement. Furthermore, floating the thin-oxide gate mitigated regenerative bipolar degradation while having a faster lateral PNP trigger, resulting in the best case of on-resistance at all current levels. The insights developed in this work help to design compact high-voltage PNPs.

5B – PI (Process Integration)
Wednesday, March 29, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency I-II-III

09:15 a.m.
5B.1 - Reliability Characterization of HBM Featuring HK+MG Logic Chip with Multi-Stacked DRAMs, Sungmock Ha: Memory Division, Samsung Electronics, Hwasung, Republic of Korea, S. Lee, G. H. Bae, D. S. Lee, S. H. Kim, B. W. Woo, N.-H. Lee, Y. S. Lee, S. Pae: Memory Division, Samsung Electronics, Hwasung, Republic of Korea

With the growth of high-speed computing memory, the HBM (High Bandwidth Memory) has been developed using advanced process technologies including high-k and metal gate process for the interfacing logic chip and 3D DRAM stack structures with TSV connections. This paper reviews overall reliability of the advanced HBM with 17nm DRAM process from device level to product level. This includes the product aging focused on logic buffer die and environmental reliability of the integrated multi-layer structure. Intrinsic FEOL and BEOL reliability such as TDDB, NBTI and EM were demonstrated >10 years of lifetime. Ni/Cu UBM (Under Bump Material) improved EM lifetime by 15x compared to the previous Ni UBM In addition, a novel package test method considering mechanical stress on 2.5D SiP (silicon in package) enabled the interconnect reliability including TSV/micro bump EM and package environmental tests level to be evaluated more precisely. Reliability of HBM with 17nm high-k metal gate process showed robustness and meets 10yrs lifetime with HTOL over 1000hrs aging, hot temperature storage, temperature humidity bias and precondition including multiple cycles of IR reflow for production.

09:40 a.m.

5B.2 - Impact of Gate Stack Thermal Budget on NBTI Reliability in Gate-All-Around Nanosheet P-Type Devices, Huimei Zhou, Miaomiao Wang, Nicolas Loubet, Andrew Gaul, Yasir Sulehria: IBM Research, 257 Fuller Road, Albany, NY 12203, USA

NBTI impact from gate stack thermal budget in Gate-All-Around Nanosheet (GAA NS) architecture is presented in this work. Varying effects of post high-k deposition anneal (PDA), spike-anneal (SA), and laser annealing (LSA) are studied in terms of the NBTI-induced threshold voltage shifts. It is observed that the NBTI, gate leakage, and mobility are significantly modulated by interfacial layer (IL) formation and Nitrogen (N) concentration from varying annealing and thermal budget. Optimized thermal process is identified to improve NBTI reliability without mobility and gate leakage degradation.

10:05 a.m.

5B.3 - Characterization and Modeling of DCR and DCR Drift Variability in SPADs, M. Sicre: TR&D, STMicroelectronics, Crolles, France; INL, UMR, CNRS 5270, Université de Lyon, Villeurbanne, France; CEA-Leti, Univ. Grenoble Alpes, F-38000 Grenoble, France, X. Federspiel, B. Mamdy, D. Roy: TR&D, STMicroelectronics, Crolles, France, F. Calmon: INL, UMR, CNRS 5270, Université de Lyon, Villeurbanne, France

A quadratic relationship between the Dark Count Rate drift (ΔDCR) device-to-device variance $\sigma^2_{\Delta DCR}$ and its mean ΔDCR regardless of stress conditions, architectures, and processes, is demonstrated in Single-Photon-Avalanche Diodes (SPADs). An Empirical Monte-Carlo method accounting for the stochastic diffusion of carriers in computation of the avalanche breakdown probability coupled with a nonradiative multiphonon-assisted carrier capture/emission rate (NRM) are used to simulate DCR at each defect site. Temperature measurements and simulations at different voltages allow capturing potential defect positions in the device. Convolution of uniform position distributions of uncorrelated individual defects Poisson-distributed in number from device-to-device accurately simulates the measured ΔDCR distributions and the $\sigma^2_{\Delta DCR}$ against ΔDCR quadratic trend along stress time.

5C – SR (System Electronics Reliability)
Wednesday, March 29, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency IV-V-VI

09:15 a.m.
5C.1 - Risk Management Informed by an Uncertain Bathtub Curve (Invited), Jason Jopling; Logic Technology Development Quality and Reliability, Intel Corporation

The standard visualization of the bathtub curve has long served as the touchstone for introducing and establishing foundational concepts of reliability life distributions and approaches to in-field risk management. This visualization, however, has remained static and become unrepresentative relative to risk factors on modern semiconductor processes, processors, and systems. This paper will revisit the conceptual bathtub curve through the lens of realities and uncertainties relevant to contemporary applications and discuss implications to risk management methods such as qualification and modeling.

09:40 a.m.
5C.2 - A Pragmatic Network-Aware Paradigm for System-Level Electromigration Predictions at Scale, Houman Zahedmanesh, Philippe Roussel, Ivan Ciofi, Kristof Croes: Reliability Expertise Center, imec, Leuven, Belgium

The standard approach for electromigration (EM) compliance checks of CMOS systems is based on failure statistics from EM tests on single isolated interconnects. Thus, when applied to interconnect schemes with parallel connections, important phenomena such as current redirection due to redundancy, are ignored. In this study, a practical network-aware paradigm is proposed to rectify this shortcoming. Benchmarking against the standard approach for a power delivery network (PDN), indicates that an order of magnitude higher standard-cell (SC) currents would be allowed due to redundancy and a failure criterion inspired by SCs optimal operation instead of single interconnect R-shift.

10:05 a.m.
5C.3 - Estimation of SOH Degradation of Coin Cells Subjected to Accelerated Life Cycling with Randomized Cycling Depths and C-Rates, Pradeep Lall, Ved Soni: Auburn University, NSF-CAVE3 Electronics Research Center, Department of Mechanical Engineering, Auburn, AL, 36849, Guneet Sethi, Kok Yiang: Amazon Lab 126, Sunnyvale, CA

Investigation of li-ion battery state of health (SOH) degradation and its modeling facilitates the determination of device warranty and can provide information about the device battery's health. For such studies, batteries undergo life-cycling tests with fixed cycling depths and charging currents (C-rates) across cycles, and the gathered degradation data is used for model development. However, in the real world, the cycling depth is generally not constant per cycle and varies across users. The SOH estimation of such use cases is challenging for lab-developed models. In this study, a semi-empirical SOH estimation regression model has been trained using fixed cycling depth and c-rate data and is validated using tests with randomized cycling depth and c-rate variation per cycle. Different upper and lower state of charge (SOC) limits were chosen to simulate different user profiles. Finally, multiple iterations of this model with different predictor variables have been tested to minimize the estimation error.

Break
Wednesday, March 29, 10:30 a.m. – 10:50 a.m. PDT

6A –EM (Emerging Memory)
Wednesday, March 29, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency Main

10:55 a.m.
6A.1 - Novel Operation Scheme for Suppressing Disturb in HfO2-Based FeFET Considering Charge-Trapping-Coupled Polarization Dynamics, Takamasa Hamai, Kunifumi Suzuki, Reika Ichihara, Yusuke Higashi, Yoko Yoshimura, Kiwamu Sakuma, Kensuke Ota, Kota Takahashi, Kazuhiro Matsuo, Shosuke Fujii, Masumi Saitoh: Institute of Memory Technology, R&D, Kioxia Corporation, Yokkaichi, Japan

We successfully demonstrate a significant suppression of the Vth shift caused by the program/erase disturb in HfO2-based ferroelectric FET (FeFET) using a novel operation scheme. Polarization reversal is found to occur after volatile carrier trapping at the HfO2/SiO2 interface. Dividing the disturb stress into a train of short voltage pulses with intentional long intervals decouples the carrier trapping from the polarization reversal. Consequently, the immunity to disturbance is improved by more than four orders of magnitude. We model the disturb suppression mechanism as follows: insufficient interfacial charge trapping unstabilizes the reversed polarization to keep the domain undisturbed. Our findings show a promising guideline for improving the reliability of the FeFET array operation.

11:20 a.m.
6A.2 - The Role of Defects and Interface Degradation on Ferroelectric HZO Capacitors Aging, Francesco Maria Puglisi; Dipartimento di Ingegneria "Enzo Ferrari", University of Modena and Reggio Emilia, Via P. Vivarelli 10, 41125 Modena, Italy, Lorenzo Benatti, Sara Vecchi: DIEF, Università di Modena e Reggio Emilia,

Via P. Vivarelli 10/1, 41125 Modena, Italy, Milan Pešic: Applied Materials Inc. 3050 Bowers Avenue, Santa Clara, CA, USA

The discovery of ferroelectricity in HfO2-based materials, especially Hf0.5Zr0.5O2 (HZO), opened to a wide range of applications. In fact, innovative HZO memories, such as ferroelectric tunnel junctions (FTJs), are suitable candidates as ultra-low power storage/synaptic elements, holding the data as a polarization state. Yet, a clear link between the device degradation and material/interface properties is still lacking. In this work, we elucidate the degradation dynamics in metal-HZO-metal (MFM) capacitors by combining ab-initio calculations, physics-based simulations, dedicated experiments, and custom data analysis based on a recently introduced small-signal device model. Stress/measure experiments are conducted to: i) extract the 2Pr (remnant polarization) evolution throughout device lifetime (from pristine to wake-up and fatigue); ii) determine parasitic series impedance and key material properties through a small-signal model; iii) evaluate the leakage current. Including the contribution of the parasitic series impedance in physics-based simulations allows reproducing leakage profiles and their cycling evolution. The combination of the proposed approaches allows to better interpret the behavior of these devices and retrieve the key role of process conditions (specifically post-deposition steps) in determining the device lifetime and overall reliability.

11:45 a.m.
6A.3 - MTJ Degradation in Multi-Pillar SOT-MRAM with Selective Writing, Simon Van Beek, Kaiming Cai: Imec, Kapeldreef 75, 3001 Leuven, Belgium, Kaiquan Fan: ESAT, KU Leuven, 3001 Leuven, Belgium, Giacomo Talmelli, Anna Trovato, Nico Jossart, Siddharth Rao, Adrian Chasin, Sebastien Couet: Imec, Kapeldreef 75, 3001 Leuven, Belgium

In SOT-MRAM, the writing path is decoupled from the reading path and therefore considered robust against MgO breakdown in the MTJ. At operation, high current densities flow through the thin metallic SOT track underneath the MTJ, causing significant heating of both the track and MTJ. At these elevated temperatures, diffusion mechanisms can cause failure of the MTJ. We find that longer tracks heat up more and can sustain less SOT current.

Moreover, applying a voltage (V_G) on the MTJ during SOT stress can cause MgO breakdown before failure by diffusion occurs. With a failure model, we can predict that breakdown event. This is particularly important in multi-pillar concepts that consist of longer tracks and use V_G for selectivity.

12:10 p.m.
6A.4 - Comprehensive Study on Prediction of Endurance Properties from Breakdown Voltage in High-Reliable STT-MRAM, H. Sato, H. M. Shin, H. Jung, S. W. Lee, H. Bae, H. Kwon, K. H. Ryu, W. C. Lim, Y. S. Han, J. H. Jeong, J. M. Lee, D. S. Kim, K. Lee, J. H. Lee, J. H. Park, Y. J. Song: R&D Center, Samsung Electronics Co., Hwaseong-si, Korea, Y. Ji, B. I. Seo, J. W. Kim, H. H. Kim: Foundry Business, Samsung Electronics Co., Yongin-Si, Korea

We have comprehensively studied prediction of endurance properties STT-MRAM based on breakdown voltage. First, by using 8Mb test MRAM chip, we clarified that a scale parameter dominating the endurance properties can be well predicted from breakdown voltage (BV) by taking into account a field acceleration parameter. We have also clarified that the field acceleration parameter can be determined by dependence of BV on a voltage sweep rate. Those results indicate that the BV measurements can be used to predict the endurance properties. Based on the results for 8Mb test chip, we have fabricated 44Mb STT-MRAM for buffer memory usage in CMOS image sensor and verified high enough endurance greater than 10^{10} cycles.

6B – PK (Packaging and 2.5/3D Assembly)
Wednesday, March 29, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency I-II-III

10:55 a.m.

6B.1 - Cross-Coupled Self-Heating and Consequent Reliability Issues in GaN-Si Hetero-Integration: Thermal Keep-Out-Zone Quantified, M. P. Sruthi: Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 United States; Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai - 600036, India, M. Asaduz Zaman Mamun: Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 United States, Deleep R. Nair, Anjan Chakravorty, Nandita Das Gupta, Amitava Das Gupta: Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai - 600036, India, Muhammad Ashraful Alam: Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906 United States

Three-dimensional (3D) hetero-integration (HI) allows Moore's law to be extended by integrating multiple materials and device technologies onto a single platform, thereby increasing the device density, performance, and functionality. 3D-HI unlocks new circuit applications and capabilities, for instance, by combining III-V devices with high-density and low-cost silicon digital control circuits. However, typically the design processes of such HI systems focus on process or performance considerations without accounting for cross-coupled reliability. We assert that the 3D-HI design would be suboptimal unless we explicitly account for the reliability issues emerging from, for example, the cross-coupled self-heating effects (SHE) that can pose severe reliability challenges of such hetero-integrated circuits. As such, we (i) propose a thermal model to predict the maximum temperature (T_{max}) attained by Si devices that are heterogeneously integrated with a hot GaN power transistor, (ii) derive an analytical model to define thermal keep-out-zone (T-KOZ) between different devices, and (iii) demonstrate how reliability issues in Si transistor, such as negative bias temperature instability (NBTI), hot carrier injection (HCI) and interconnect electromigration (EM) can be mitigated by carefully selecting the substrate material and implementing forced cooling. The method is generic and can be tailored for any arbitrary combination of technologies.

11:20 a.m.

6B.2 - Reliability Challenges from 2.5D to 3DIC in Advanced Package Development, Ryan Lu, Yao-Chun Chuang, Jyun-Lin Wu, Jun He: Quality and Reliability, Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Taiwan, R.O.C.

Advanced packaging platforms such as 3DIC and 3D Fabric have encountered increased reliability risks with advanced packaging architectures such as CoWoS (Chip on Wafer on Substrate), InFO (Integrated Fan Out), SoIC (System on Integrated Chips). Material analysis, mechanical, and board/system level reliability tests were conducted to reduce reliability concerns and improve the robustness of 3DIC architecture. To further evaluate the lifetime of these architectures the new extended test duration is implemented. Using the previously mentioned novel testing approaches, technology development can be rapidly improved, and a reference design can be created to meet requirements of customers' products in the future.

6C – GaN (GaN Power Device)
Wednesday, March 29, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency IV-V-VI

10:55 a.m.

6C.1 - Drain Voltage Impact on Charge Redistribution in GaN-on-Si E-Mode MOSc-HEMTs, C. Leurquin, W. Vandendaele, R. Gwoziecki, B. Mohamad, G. Despesse: Université Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France, F. Iucolano, R. Modica: Research and Development Department, STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy, A. Constant: Research and Development Department, STMicroelectronics, 10 Rue Thalès de Millet, 37100, Tours, France

In this paper, we review the nature of traps population and the transport mechanisms in GaN-on-Si E-mode MOS channel HEMTs during High Voltage Bias Temperature Instabilities (HV-BTI) test under various temperatures (T),

drain voltage stress ($V_{DSstress}$) and gate voltage stress ($V_{GSstress}$) conditions. Thanks to experimental setup using ultra-fast Id(V_g) to monitor VTH during both stress and recovery phases from 10μs to several kiloseconds. The temperature dependent measurements show that V_{th} and Ron degradations are related to the Cn deep acceptor traps in GaN:C layer. Two mechanisms during the stress phase are identified, Cn traps deionization first, impacted by $V_{DSstress}$, then nBTI behavior influenced by $V_{GSstress}$. It is observed that high drain voltage stress ($\geq$ 200V) induces a charge redistribution predominantly towards the drain node, while a lower drain voltage stress led to a charge redistribution in the source-gate region.

11:20 a.m.
6C.2 - Dielectric Thickness and Fin Width Dependent OFF-State Degradation in AlGaN/GaN SLCFETs, Akhil S. Kumar, Michael J. Uren, Matthew D. Smith, Martin Kuball: Center for Device Thermography and Reliability, University of Bristol, Bristol BS8 1TL, U.K., Justin Parke, H. George Henry, Robert S. Howell: Northrop Grumman Mission Systems, Linthicum, MD 21090, USA

Accelerated OFF-State stressing of multichannel AlGaN/GaN Superlattice Castellated Field Effect Transistors (SLCFET) with varying dielectric thickness (di) and fin-width (W_{fin}) was studied using noise measurements. As d_i increased, the failure mechanism changed from an abrupt breakdown to gradual time dependent dielectric breakdown (TDDB). Smaller W_{fin} is found to extend lifetime compared to wider W_{fin} under such stressing condition. Percolation theory and associated trap generation during stressing can explain the observed behavior.

11:45 a.m.
6C.3 - Unique Lattice Temperature Dependent Evolution of Hot Electron Distribution in GaN HEMTs on C-Doped GaN Buffer and its Reliability Consequences, Rajarshi Roy Chaudhuri, Vipin Joshi, Amratansh Gupta, Tanmay Joshi, Rasik Rashid Malik, Mehak Ashraf Mir, Sayak Dutta Gupta, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India

Through this work, a unique substrate temperature dependent evolution of hot electron distribution is reported in GaN HEMTs on C-doped GaN buffer, and its reliability consequences are discussed. With rise in substrate temperature, significant rise in hot electron concentration, its energy, and interaction with buffer traps is observed at the drain edge, in contrast to an expected reduction in hot electron population. A mechanism based on carrier de-trapping and transport to drain is proposed and experimentally validated.

12:10 p.m.
6C.4 - Dynamic Interplay of Surface and Buffer Traps in Determining Drain Current Injection Induced Device Instability in OFF-State of AlGaN/GaN HEMTs, Mehak Ashraf Mir, Vipin Joshi, Rajarshi Roy Chaudhuri, Mohammad Ateeb Munshi, Rasik Rashid Malik, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, India

Through detailed experiments and computations, this study reveals a complex interplay of surface and buffer traps in determining AlGaN/GaN HEMT device's response to an OFF-state drain current injection stress. A time dependent drain voltage build-up is observed in the devices, followed by a gradual reduction for a drain current injection of a few nA. The process of voltage build-up is found to be assisted by channel depletion driven by dynamic trapping in the buffer acceptor traps, while the fall in voltage is caused by channel turn ON driven by trap ionization of the surface donors. Moreover, the current injection induced drain voltage build-up also resulted in a significant increase in the dynamic ON resistance of the device.

Break
Wednesday, March 29, 12:00 p.m. – 01:30 p.m. PDT

7A – CR (Circuit Reliability and Aging)
Wednesday, March 29, 01:40 p.m. – 03:00 p.m. PDT
Venue: Regency Main

01:45 p.m.
7A.1 - Ultra Long-Term Measurement Results of BTI-Induced Aging Degradation on 7-nm Ring Oscillators,
Kazutoshi Kobayashi, Tomoharu Kishita, Hiroki Nakano, Jun Furuta: Dept. of Electronics, Kyoto Institute of Technology, Kyoto, Japan, Mitsuhiko Igarashi, Shigetaka Kumashiro, Michitarou Yabuuchi, Hironori Sakamoto: Renesas Electronics Corporation, Tokyo, Japan

We measured ultra-long term BTI-induced degradation of 7-nm ring oscillators (ROs) using a measurement system controlled by an FPGA and a microcontroller unit. The ambient temperature and the supply voltage were set to 125° C and the nominal voltage of 0.75 V. The measurement results showed that even over a very long period around 5 months (1e7 s), the RO oscillation frequency continuously degraded with t^n. We propose a degradation model in which BTI-induced traps are increasing as time. The model can successfully replicate the continuous ever-lasting-like degradation.

02:10 p.m.
7A.2 - Modeling of NBTI Induced Threshold Voltage Shift Based on Activation Energy Maps under Consideration of Variability, Christian Bogner: Institute for Microelectronics, TU Vienna; Infineon Technologies AG, Munich, Christian Schlünder: Infineon Technologies AG, Munich, Michael Waltl: Institute for Microelectronics, TU Vienna, Hans Reisinger: Infineon Technologies AG, Munich, Tibor Grasser: Institute for Microelectronics, TU Vienna

One of the major challenges for modeling BTI degradation in modern technology nodes and deeply scaled transistors is the occurrence of significant time dependent variability (TDV). This means that due to the sparsity of defects, the impact of single defects as well as variation in the number of defects per device need to be taken into consideration. We present a modeling approach based on physical principles to describe both mean parameter degradation as well as TDV. Our approach is based on activation energy maps combined with an exponential-Poisson model in order to capture variability. For parameter extraction a combination of ultra fast measurements on large area transistors and transistor array measurements are applied. Thereby, ultra fast measurements have the capability to make a wide range of capture-/emission times experimentally accessible, improving the confidence of the extracted activation energy map. On the other hand, transistor arrays have proven to be the ideal test vehicle to efficiently measure an ensemble of transistors and to asses TDV.

02:35 p.m.
7A.3 - The Role of Mobility Degradation in the BTI-Induced RO Aging in a 28-nm Bulk CMOS Technology: (Student Paper), D. Sangani: IMEC, Kapeldreef 75, B-3001 Leuven, Belgium; Department of Electrical Engineering ESAT, Katholieke Universiteit Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium, J. Diaz-Fortuny, E. Bury, B. Kaczer: IMEC, Kapeldreef 75, B-3001 Leuven, Belgium, G. Gielen: IMEC, Kapeldreef 75, B-3001 Leuven, Belgium; Department of Electrical Engineering ESAT, Katholieke Universiteit Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium

Shrinking reliability margins have created an increasing demand for circuit aging simulations, which enable product reliability assessment pre-production. Physical Design Kits (PDKs) of modern technologies have started to include compact models for transistor degradation mechanisms along with a dedicated reliability simulation framework. In this work, we present a study of the commercial aging models in a 28-nm CMOS technology from a designer perspective by comparison of the simulations with extensive measurement data at the device and the circuit level (ring oscillators). Moreover, using our custom table model compiled from our device-level measurement data, we model the BTI-driven component of circuit-level degradation and provide convincing evidence that mobility

degradation due to NBTI plays an important role in the circuit aging phenomenon, thus emphasizing its need in SPICE-level NBTI models.

7B – RT (Reliability Testing)
Wednesday, March 29, 01:40 p.m. – 03:00 p.m. PDT
Venue: Regency I-II-III

01:45 p.m.
7B.1 - Reliability of GaN MOSc-HEMTs: From TDDB to Threshold Voltage Instabilities (Invited), W. Vandendaele, C. Leurquin, R. Lavieville, M. A. Jaud, A. G. Viey, R. Gwoziecki, B. Mohamad, E. Nowak: Université Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France, A. Constant, F. Iucolano: R&D Department, STMicroelectronics, Stradale Primosole 50,95121, Catania, Italy

In this paper, we review the gate reliability of the GaN MOSc-HEMT as well as the specific method to address the peculiarities of these transistors. The long term forward gate TDDB will be explored showing the impact of the gate recession and gate material on the expected maximum gate oxide field ($E_{OX,MAX}$) at 10 years. The gate related threshold voltage instabilities (pBTI and nBTI) are reviewed showing the interplay between epitaxy material and gate oxide process. Finally, the high drain voltage influence on V_{th} (HVBTI) is studied through the development of specific and dedicated setup allowing a deeper understanding of the device instabilities during operation.

02:10 p.m.
7B.2 - Using Dedicated Device Arrays for the Characterization of TDDB in A Scaled HK/MG Technology, P. Saraza-Canflanca, J. Diaz-Fortuny: imec, Kapeldreef 75, 3001 Leuven, Belgium, A. Vici: imec, Kapeldreef 75, 3001 Leuven, Belgium; KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven, Belgium, E. Bury, R. Degraeve, B. Kaczer: imec, Kapeldreef 75, 3001 Leuven, Belgium

The impact of Time-Dependent Dielectric Breakdown (TDDB) on scaled technologies' reliability has regained interest in the last years. Due to the stochastic nature of TDDB, its characterization must be performed in a statistically-significant manner, i.e., involving a large number of devices. In this paper we present an array fabricated in a 28 nm, HK/MG commercial technology that contains more than 30,000 test devices. We demonstrate its adequacy for the study of TDDB through several tests, including TDDB stress on NMOS and PMOS devices biased in inversion and accumulation modes.

7C – RE (Radiation Effect Reliability)
Wednesday, March 29, 01:40 p.m. – 03:00 p.m. PDT
Venue: Regency IV-V-VI

01:45 p.m.
7C.1 - Soft- and Hard-Error Radiation Reliability of 228 KB 3T+1C Oxide Semiconductor Memory, H. Takahashi: NOS Development Division, 398 Hase, Atsugi, Kanagawa 243-0036, Japan, Y. Okamoto: CAD Division Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa 243-0036, Japan, T. Hamada: NOS Development Division, 398 Hase, Atsugi, Kanagawa 243-0036, Japan, Y. Komura: CAD Division Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa 243-0036, Japan, S. Watanabe, K. Tsuda, H. Sawai: NOS Development Division, 398 Hase, Atsugi, Kanagawa 243-0036, Japan, T. Matsuzaki: CAD Division Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa 243-0036, Japan, Y. Ando, T. Onuki, H. Kunitake, S. Yamazaki: NOS Development Division, 398 Hase, Atsugi, Kanagawa 243-0036, Japan, D. Kobayashi, A. Ikuta: Institute of Space and Astronautical Science, Japan Aerospace Exploration Agency, 3-1-1 Yoshinodai, Chuo, Sagamihara, Kanagawa 252-5210, Japan, T. Makino, T. Ohshima: Quantum Materials and Applications Research Center, National Institutes for Quantum Science and Technology, 1233 Watanuki, Takasaki, Gumma 370-1207, Japan

We prototyped a 228 KB oxide semiconductor memory utilizing field-effect transistors with a c-axis-aligned crystalline oxide semiconductor (CAAC-OSFETs) and evaluated its tolerance to hard errors caused by X-rays and soft errors caused by heavy-ion beams. Evaluation results demonstrate that the OS memory has radiation tolerance high enough to operate properly even in space radiation environments.

02:10 p.m.
7C.2 - Soft Error Rate Predictions for Terrestrial Neutrons at the 3-nm Bulk FinFET Technology, Yoni Xiong: Vanderbilt University, Nashville, TN, USA, Yueh Chiang: Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, Nicholas J. Pieper, Dennis R. Ball, Bharat L. Bhuva: Vanderbilt University, Nashville, TN, USA

Soft error rates are predicted for the 3-nm bulk FinFET technology node using layout-informed Geant4 simulations and experimental data from the previous 7-nm and 5-nm bulk FinFET nodes. Single-event hit current and voltage transient characteristics are analyzed with literature-based models at the 7-nm, 5-nm, and 3-nm bulk FinFET nodes.

02:35 p.m.
7C.3 - Scaling Trends and the Effect of Process Variations on the Soft Error Rate of Advanced FinFET SRAMs, B. Narasimham, H. Luk, C. Paone, A-R. Montoya, T. Riehle, M. Smith, L. Tsau: Broadcom Inc, Irvine CA USA

Scaling trends in the alpha-particle and neutron induced SRAM SER shows an increase in the per-bit SER and percent multi-cell upsets at the 5-nm FinFET process compared to the 7-nm process. Neutron SER tests across process corners show that the faster process corner SER is up to 2× higher than the slower process corner SER in 7-nm and 5-nm FinFETs. The process corner dependence of SER is attributed to differences in propagation delay and single-event transient pulse-widths.

Break
Wednesday, March 29, 03:00 p.m. – 03:20 p.m. PDT

8A – TX (Transistors)
Wednesday, March 29, 03:20 p.m. – 05:40 p.m. PDT
Venue: Regency Main

03:25 p.m.
8A.1 - Reliability Assessment of 3nm GAA Logic Technology Featuring Multi-Bridge-Channel FETs, Seongkyung Kim, Hyerim Park, Eunyu Choi, Young Han Kim, Dahyub Kim, Hyewon Shim, Shinyoung Chung, Paul Jung: Samsung Foundry Business, Samsung Electronics, Hwaseong si, Republic of Korea

In this paper, we report reliability assessment of the Multi-Bridge-Channel FET (MBCFET) adopted 3nm gate all around (GAA) logic technology in comparison with the 4 and 8nm FinFET logic technologies. A notable improvement on negative bias temperature instability (NBTI) of MBCFET is observed thanks to {100} dominance. Gate oxide time-dependent-dielectric-breakdown (TDDB) of the 3nm MBCFETs is comparable to that of the 4nm and 8nm FinFETs. Self-heat decoupled hot-carrier-injection (HCI) is similar to that of the 4nm FinFETs. Reduced conductance maximum ($G_{m,max}$) indicates that HCI degradation of the 3nm MBCFETs is dominated by interface damage mechanism. Middle-of-the-line (MOL) TDDB Weibull distribution shows that the 3nm MBCFETs have shorter time-to-failure (TTF) due to reduced lateral distance from gate to diffusion contact than other FinFET logic technologies. Due to an adoption of self-aligned-contact (SAC), the 3nm MBCFETs have similar behavior on MOL breakdown voltage (Vbd) at various diffusion contact misalignment to the 4nm FinFETs. The 3nm MBCFETs show

antenna immunity up to 3× antenna ratio. Lastly, thermal cycle (TC) results indicate that the 3nm GAA logic technology has little lattice-related defects.

03:50 p.m.
8A.2 - Localized Thermal Effects in Gate-All-Around Devices, Colin Landon: Logic Technology Development, Intel Corporation, Hillsboro, USA, Lei Jiang: Logic Technology Development, Intel Corporation, Hillsboro, USA, Daniel Pantuso: Logic Technology Development, Intel Corporation, Hillsboro, USA, Inanc Meric, Kam Komeyli, Jeffrey Hicks, Daniel Schroeder: Corporate Quality Network, Intel Corporation, Hillsboro, USA

Gate-all-around (GAA) devices continue the technology trends of increased localized thermal confinement and higher performance. We describe the methodology used for localized thermal analysis and data collection of temperature rise on the transistor scale and compare GAA cell thermal resistance to Fin-FET cells. We demonstrate that the implications of GAA on device temperature are not a constraint to realizing the full technology benefits with proper thermal management.

04:15 p.m.
8A.3 - Reliability challenges in Forksheet Devices, E. Bury, M. Vandemaele, J. Franco, A. Chasin, S. Tyaginov, A. Vandooren, R. Ritzenthaler, H. Mertens, J. Diaz Fortuny, N. Horiguchi, D. Linten, B. Kaczer: imec, Kapeldreef 75, 3001 Leuven, Belgium

The forksheet (FSH) device architecture is a possible candidate towards continued logic cell downscaling. It consists of vertically stacked n- and p- type sheets at opposing sides of a dielectric wall. In this work, we overview the time-0 and time-dependent performance of n and p-type FSH field-effect transistors co-integrated with nanosheets (NSH) in individual wafers. A separate assessment of dedicated capacitors yields indications of a non-negligible effect of negative fixed charges trapped in low-temperature deposited SiO_2, currently used as dielectric wall liner. Finally, we evaluate the impact of using a bottom dielectric isolation (BDI) instead of a junction-based electrical isolation of the sheets from the substrate.

Break
Wednesday, March 29, 04:40 p.m. – 04:50 p.m. PDT

04:50 p.m.
8A.4 - Unveiling Field Driven Performance Unreliabilities Governed by Channel Dynamics in MoSe2 FETs, Utpreksh Patbhaje, Rupali Verma, Jeevesh Kumar, Ansh Shrivastava, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India

MoSe2 is a wonderful ambipolar 2D material that provides a great platform for future electronics but lacks analysis for operation under electrical stress. This work focuses on parameter drifts observed in MoSe2 FETs due to evolution of channel as function of time and applied field during which captured stress current shows increment trends that does not saturate even after 1000 seconds of operation. ID(max) improvement of 42%, VT shifts by 380%, SS improvement by 30% and mobility increment by 33% presents unreliable scenarios in operation. This has been attributed to persistent strain in channel that manifests as improved ordering in channel that points to contact region being susceptible to performance degradation in MoSe2 FETs.

05:15 p.m.
8A.5 - A Unified Framework to Explain Random Telegraph Noise Complexity in MOSFETs and RRAMs, Sara Vecchi, Paolo Pavan, Francesco Maria Puglisi: Dipartimento di Ingegneria "Enzo Ferrari", Via P. Vivarelli 10/1, 41125 - Modena (MO) – Italy; Università degli Studi di Modena e Reggio Emilia

As well known, the implementation of high-κ dielectrics (e.g., HfO2) in nanoscale devices is unavoidable to cope with the device scaling required by the market. Nevertheless, due to the higher defect density compared to SiO2,

hafnium oxide exhibits stronger and more complex Random Telegraph Noise (RTN), namely one of the most relevant defect-related reliability issues in ultra-thin oxides. However, depending on the device type, HfO2 can be characterized by different defect density and therefore leading to a different RTN signals. In particular, in Resistive Random Access Memory (RRAM) devices RTN arises very often but shows a high degree of complexity (e.g., multilevel, anomalous, temporary RTN) and instabilities [3,4] which hinders its characterization. Conversely, in MOSFETs RTN has a small occurrence and it typically exhibits a simple behavior (i.e., 2-level signal) if detected. In this work, we fully analyze such phenomena in different devices providing a unified and physics-based framework which is also confirmed by experiments. The results of this study will be crucial for the design of new devices and circuits for emerging RTN-based applications, such as True Random Number Generators (TRNGs).

8B – FA (Failure Analysis)
Wednesday, March 29, 03:20 p.m. – 05:40 p.m. PDT
Venue: Regency I-II-III

03:25 p.m.
8B.1 - Advanced Methods of Detecting Physical Damages in Packaging and BEOL Interconnects, Jorge Mendoza, Jimmy-Bao Le, Choong-Un Kim: Materials Science and Engineering, University of Texas at Arlington, Arlington, TX, Hung-Yun Lin: Texas Instruments, Inc., Dallas, Texas 75243

This paper reports new methods of detecting damages and failures in packaging interconnects in fully packaged devices with sufficient sensitivity and selectivity for damages in interconnects. Exploration on various electrical methods leads to the conclusion that a few electrical measurement techniques, especially one using a low frequency AC signal, may provide effective mechanism of detecting the damages under interest. Impedance and derived parameters such as capacitance and inductance show sensitivity to silicon-package-interaction damages, with satisfactory immunity to parasitic signals present in fully assembled/packaged test chips such as the probe/pad contact resistance and stray capacitance from various sources. Two highlighting examples based on the "open circuit test pattern" are introduced in this paper to demonstrate the effectiveness of developed methods. The first is the damage detection in the high resistance open circuit pattern, which consists of small metal serpentines strategically placed on the failure prone places in BEOL of Si chip. Small damage develop in the metal serpentine makes the circuits to produce LC resonance-like signals useful in detecting presence of damage and its location. The second is the impedance method sensitive to the damage/failure in low resistance open circuit pattern like solder interconnects. The method measures the impedance as a function of frequency and design to detects the crack and/or void trapped/developed at the solder joints mainly using the skin effect in AC resistance. The technique is with its own limitations but can enable effective characterization of damages in package interconnects.

04:15 p.m.
8B.3 - Investigation of Sub-20nm 4th Generation DRAM Cell Transistor's Parasitic Resistance and Scalable Methodology for Sub-20nm Era, Shinwoo Jeong, Jin-Seong Lee, Jiuk Jang, Jooncheol Kim, Hyunsu Shin, Ji Hun Kim, Jeongwoo Song, Dongsoo Woo, Jeonghoon Oh, Jooyoung Lee: DRAM Product & Technology, Samsung Electronics Co, Pyeongtaek, 17786, Korea

Break
Wednesday, March 29, 04:40 p.m. – 04:50 p.m. PDT

The component of cell parasitic resistance at sub-20nm 4th generation DRAM cell transistor is investigated. To evaluate the cell characteristics, the Gate Buried Contact (GBC) to Active contact formation method with varied dopant concentrations was studied. We have discovered a scalable methodology that simultaneously reduces parasitic resistance and leakage with regard to Gate Induced Drain Leakage (GIDL). Also, we proved the importance of interface quality of Direct Contact on Cell (DCC) in order to reduce the parasitic resistance. The failure analysis is conducted by segmenting the resistance with Test Element Groups (TEGS) at wafer level. And the process

windows and local variations from fabricated devices are electrically verified by core failure analysis. Through this investigation, we proposed the scalable methodology that can sustain generational scalability of DRAM.

04:50 p.m.
8B.4 - Analysis of Intermittent Single-Bit Failure on 10-nm Node Generation DRAM Devices, Hyewon Seo, Taiuk Rim, Eunsun Lee, Sekyoung Jang, Kyosuk Chae, Jeonghoon Oh, Hyodong Ban, Jooyoung Lee: DRAM Product & Technology, Memory Business, Samsung Electronics, Hwaseong-si, Gyeonggi-do, Republic of Korea

The intermittent single-bit (SB) failure is one of the most important problems in DRAM technology development because it is almost impossible to reproduce and screen out. In this paper, the intermittent SB failure was analyzed theoretically. Based on our physical modeling, we suggested several technical methods to reduce the intermittent SB failure and got the experimental results that decrease the intermittent SB failure rate. Furthermore, we predicted the failure rate based on our theoretical model. The SB failure rate had over 85% consistency between prediction and results. Therefore, we proved that our failure modeling is appropriate for predicting the occurrence of the intermittent SB failure. Furthermore, we can propose the design of the next generation DRAM technology to achieve equivalent or better intermittent SB quality than the previous generation from the beginning of the development.

05:15 p.m.
8B.5 - Microscopic Characterization of Failure Mechanisms in Long-Term Implanted Microwire Neural Electrodes, Z. J. Zhang: Shanghai Key Laboratory of Multidimensional Information Processing, East China Normal University, Shanghai, China, Q. Li: Shanghai Key Laboratory of Brain Functional Genomics (Ministry of Education), School of Life Sciences, East China Normal University, Shanghai, China, Z. Y. Dong, W. T. Wang, S. T. Lai, X. Yang, F. Liang, C. L. Wang, C. Luo, L. J. Lyu, Z. Li: Shanghai Key Laboratory of Multidimensional Information Processing, East China Normal University, Shanghai, China, J. M. Xu: Shanghai Key Laboratory of Brain Functional Genomics (Ministry of Education), School of Life Sciences, East China Normal University, Shanghai, China, X. Wu: Shanghai Key Laboratory of Multidimensional Information Processing, East China Normal University, Shanghai, China

The development of integrated circuits greatly enhances brain-computer interface technology. The degradation of the implanted neural electrodes is a key issue. The scanning electron microscope and energy dispersive spectrometer techniques are used to characterize the evolution of the microscopic morphology and element migration of implanted microwire electrodes containing 32 channels together with the recorded neural signals at different implantation times. The spike amplitude decreases over time of implantation, leading to poorer identification of neural signals. The effect of degradation on the local field potential detection is neglectable. This work could guide the reliability improvement of the neural electrodes.

8C – RF (RF/mmW/5G)
Wednesday, March 29, 03:20 p.m. – 05:40 p.m. PDT
Venue: Regency IV-V-VI

03:25 p.m.
8C.1 - Differentiated Silicon Technologies for mmwave 5G and 6G applications (Invited), Anirban Bandyopadhyay: GLOBALFOUNDRIES Inc., Smart Mobile Devices & Wearables, 2600 Great America Way, Santa Clara, California, USA

The mobile broadband (MBB) connectivity based on 4G and 5G cellular connectivity has enabled high data throughput and low latency applications on smart mobile devices. The enhanced MBB (eMBB) using 5G particularly mmwave frequency bands has the capability of further enhancing data rate to true multi-Gb/s. While mmwave (24-52GHz) allows huge channel bandwidth to enable enhanced broadband, it also poses a lot of technical

challenges in terms of coverage, efficient generation of transmitted power particularly in the uplink, system cost and long-term reliability of the hardware system. In future, carrier frequencies will go even higher to >100GHz particularly D-band (120-160GHz) for both communication and sensing. This paper highlights the hardware challenges for sub 6GHz, mmwave and sub-THz radio and performance limits of semiconductor technologies particularly CMOS compared to different compound semiconductor technologies.

03:50 p.m.
8C.2 - Reliability of SPST Series-Stacked SOI CMOS RF Switches for mmWave Applications, Aarti Rathi, Abhisek Dixit: Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India, Naga Satish: Quality and Reliability Engineering, Bangalore, India, P. Srinivasan, Fernando Guarin: Quality and Reliability Engineering, GLOBALFOUNDRIES Inc., Malta, US

In this work, we have investigated the reliability degradation mechanisms in RF switches for 45nm RFSOI technology under DC and RF stress modes. We have used singlepole single-throw RF switches using thin and thick gate oxide in series stacked configurations using $R_{ON} \cdot C_{OFF}$ as a key metric. Degradation and breakdown depend on stress time, DC gate and drain voltages, and RF power. The mechanism causing degradation is studied using the voltage swings at the terminals of the RF switch. In addition, stress recovery is also observed in some cases, which is critical for switches used in transceivers. Overall, the switch exhibits superior reliability under RF 5G mmWave operating conditions.

04:15 p.m.
8C.3 - RF Long Term Aging Behavior and Reliability in 22FDX WiFi Power Amplifier Designs for 5G Applications, P. Srinivasan, J. Lestage, S. Syed, X. Hui, S. Moss, O. D. Restrepo, O. H. Gonzalez, Y. Chen, T. McKay, A. Bandyopadhyay, N. Cahoon, F. Guarin, B. Min, M. Gall: GLOBALFOUNDRIES, 400 Stone Break Road Extension, Malta NY, USA 12020, S. Ludvik: Power Technology Solutions, Palo Alto, CA, USA

RF long term aging and large signal reliability in 22FDX Wi-Fi Power Amplifier (PA) designs is investigated. Packaged PA operating at 5.4GHz, 3.3V V_{DD} with LDMOS as Common Gate and SLVT as Common Source is stressed under accelerated DC and RF power conditions for +1.5kPOH at T_A=25 C. A custom built Power Amplifier Test System (PATS) tool capable of large signal on packaged samples is used for long term stress. Initial RF performance of ∼26 dBm, with gain 14∼15 is seen before stress. Power sweeps at regular stress intervals were performed to validate PA degradation. Self-heating effect is studied by correlating T_A to junction temp T_j using thermal models. Thermal images confirm that higher Pdiss leads to higher T_j. Output power degradation of < 0.5dB is seen at accelerated voltage of 4.2V after +1.5kPOH which is correlated to voltage swings. Key limiting mechanism for common gate and source devices are identified, demonstrating the viability of CMOS FDSOI technology for 5G applications.

Break
Wednesday, March 29, 04:40 p.m. – 04:50 p.m. PDT

04:50 p.m.
8C.4 - Impact of Non-Conducting HCI Degradation on Small-Signal Parameters in RF SOI MOSFET, Dora A. Chaparro-Ortiz, Alan Y. Otero-Carrascal, Edmundo A. Gutiérrez-D., Reydezel Torres-Torres: Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE), Electronics Department, Tonantzintla, Mexico, Oscar Huerta-Gonzalez, P. Srinivasan, Fernando Guarín: GlobalFoundries Inc., Malta, NY, USA

DC curves and S-parameters up to 30 GHz measured before and after hot-carrier-injection (HCI) stress in non-conducting (NC) mode are used to study the degradation suffered by the small-signal input and output impedances

of a PD-SOI MOSFET. Modeling of the gate oxide (R_{ox}) and channel resistance (R_{ch}) due to NC-HCI is also performed and investigated in detail. Noticeable impact on the device's input resistance is seen for the first time up to frequencies of 500 MHz, but it is expected to increase further into the microwave frequency range as the gate leakage increases due to either device degradation or large applied gate voltage.

05:15 p.m.
8C.5 - Thermally-Activated Failure Mechanisms of 0.25 μm RF AlGaN/GaN HEMTs Submitted to Long-Term Life Tests, Zhan Gao, Francesca Chiocchetta, Fabiana Rampazzo, Carlo De Santi, Mirko Fornasier, Gaudenzio Meneghesso, Matteo Meneghini, Enrico Zanoni: Department of Information Engineering, University of Padova, Via Giovanni Gradenigo 6B, 35131 Padova, Italy

Reliability and failure mechanism of 0.25 μm AlGaN/GaN HEMTs under thermal storage tests and high temperature operating life (HTOL) tests have been evaluated. Results show that, during thermal storage tests, Schottky metal interdiffusion and gate sinking took place, possibly accompanied by thermo-mechanical degradation, with an activation energy of 1.8 eV. Failure modes consisted in carrier density decrease and sheet resistance increase, positive V_{th} shift and Idss decrease. During HTOL tests, the degradation is mainly due to electrochemical oxidation of AlGaN, leading to on resistance increase, and Idss and gm decrease, with an activation energy of 1.0 eV.

Poster Reception - Sponsored by Qualcomm
Wednesday, March 29, 06:00 p.m. – 09:00 p.m. PDT
Venue: Monterey Ballroom

P1.CR - Enhancing Reliability of a Strong Physical Unclonable Function (PUF) Solution Based on Virgin-State Phase Change Memory (PCM), L. Cattaneo, M. Baldo, N. Lepri, F. Sancandi: Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IUNET, Piazza L. da Vinci 32, 20133, Milano, Italy, M. Borghi, E. Petroni, A. Serafini, R. Annunziata, A. Redaelli: STMicroelectronics, Via C. Olivetti 2, 20864, Agrate Brianza, Italy, D. Ielmini: Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IUNET, Piazza L. da Vinci 32, 20133, Milano, Italy

In the era of the internet of things (IoT), hardware physical unclonable functions (PUFs) have become an essential feature for authentication of any system on chip (SoC). Identifying physical entropy sources is essential for developing low-cost, low-power, highly reliable PUFs. This work presents a new PUF circuit based on embedded PCM, called MVPUF. The new PUF relies on the random virgin state of the PCM combined with a new selection technique of challenge-response pairs (CRPs), thus showing better reliability compared to PUFs based on resistive switching memory (RRAM).

P3.CR - A Physical Unclonable Function Leveraging Hot Carrier Injection Aging, Rachael J. Parker, Jyothi Bhaskarr A. Velamala, Kuan-Yueh James Shen, David Johnston: Design Engineering Group, Intel Corporation, Hillsboro, OR, U.S.A, Yao-Feng Chang, Stephen M. Ramey: Logic Technology Development Quality & Reliability, Intel Corporation, Hillsboro, OR, U.S.A., Siang-Jhih Sean Wu, Padma Penmatsa: Manufacturing and Product Engineering, Intel Corporation, Folsom, CA, U.S.A.

Physical Unclonable Functions (PUFs) are low-cost cryptographic primitives used to generate unique, secure, and stable IDs for device authentication and secure communication. PUFs rely on process variation inherent in the manufacturing flow making it impossible to predict or clone chip IDs providing a high level of security and tamper resistance. A commonly studied PUF is the memory PUF which suffers high Bit Error Rate (BER) across environmental conditions. This paper introduces a novel NFET PUF featuring a Hot Carrier Injection (HCI) stress mechanism to lower BER to near zero. Post-Si data from a 1kb PUF array fabricated in Intel4 FinFET technology is presented in comparison to a hybrid-SRAM style PUF. BER results were studied with different stress parameters enabling manufacturing flow for HCI based PUFs.

P4.CR - Characterizing BTI and HCD in 1.2V 65nm CMOS Oscillators Made from Combinational Standard Cells and Processor Logic Paths, Victor M. van Santen: Semiconductor Test and Reliability (STAR), University of Stuttgart, Stuttgart, Germany, Jose M. Gata-Romero, Juan Nunez, Rafael Castro-Lopez, Elisenda Roca: IMSE-CNM, CSIC/Universidad de Sevilla, Sevilla, Spain, Hussam Amrouch: Semiconductor Test and Reliability (STAR), University of Stuttgart, Stuttgart, Germany

Bias Temperature Instability (BTI) and Hot-Carrier Degradation (HCD) are key aging mechanisms, frequently studied with transistor measurements or inverter-based (INV) Ring Oscillators (RO) measurements. However, large-scale digital circuits are typically manufactured with standard cells (such as logic gates). In a reliability simulation flow (e.g., SPICE-based standard cell characterization with degraded transistors), many assumptions about the standard cells have to be made (such as load capacitance, signal slews, uncertainty in aging models, etc.) and can lead to high simulation uncertainty. In this work, we propose to verify this standard cell characterization with standard cell oscillator measurements in silicon. For this purpose, we present the following novel contributions: 1) The first work with BTI and HCD measurements of heterogeneous oscillators (multiple different cell types in one RO) based on logic paths extracted from processors. 2) The first work exploring the impact of BTI and HCD on oscillators containing combinational standard cells, i.e. single cells incorporating multiple logic gates (such as And-Or-Inverter (AOI) cells and Or-And-Inverter (OAI)) and cells performing complex actions such as full-adders.

P5.EM - A World First QLC RRAM: Highly Reliable Resistive-Gate Flash with Record 108 Endurance and Excellent Retention, M. Y. Li: Dept. of Electrical Engineering and Institute of Electronics, National Chiao Tung University, Taiwan, J. P. Lee, C. H. Liu: Dept. of Mechatronics Engineering, National Taiwan Normal University, Taiwan, J. C. Guo, Steve S. Chung: Dept. of Electrical Engineering and Institute of Electronics, National Chiao Tung University, Taiwan

In this paper, we demonstrated successfully a quad-level cell (QLC) of a resistive-gate memory. It was implemented in a 1k bits chip with integration of FinFET core on a mature logic platform. Comprehensive reliabilities have been examined. The results show the forming-free property, low programming current ($<\mu A$), high endurance and excellent data retention. A record high 5×10^8 endurance can be achieved. Furthermore, a 4-bit-per-cell (16 levels) has been demonstrated successfully. The chip-level performance is also analyzed, showing well disturbance-immune during SET/RESET, READ, which kept healthy signal-to-noise margin, 2-3x. This architecture is a strong candidate for the next generation resistance memory.

P6.EM - Interval Time Dependent Wake-Up Effect of HfZrO Ferroelectric Capacitor, Yaru Ding, Xinwei Yu, Chu Yan, Zeping Weng: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China, Yiming Qu, Yi Zhao: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China; School of Integrated Circuits, East China Normal University, Shanghai 200241, China.

In this work, the wake-up effect of Hf-based ferroelectric memories has been studied as a reliability concern, and related mechanisms have been proposed. By changing different waveforms, it is found that the wake-up behavior strongly depends on the interval time, and the memory window increases faster with the shorter interval time. Moreover, this difference in wake-up rate is well elaborated by the domain pinning in the non-switching region and the diffusing back defects in the switching region.

P7.EM - Cryogenic Endurance of Anti-Ferroelectric and Ferroelectric Hf1-xZrxO2 for Quantum Computing Applications, K.-Y. Hsiang: Institute and Undergraduate Program of Electro-Optical Engineering, National Taiwan Normal University, Taipei, Taiwan; Department of Electronics Engineering and Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, J.-Y. Lee: Institute and Undergraduate Program of Electro-Optical Engineering, National Taiwan Normal University, Taipei, Taiwan; Graduate School of Advance

Technology, National Taiwan University, Taipei, Taiwan, Z.-F. Lou, F.-S. Chang, Z.-X. Li: Institute and Undergraduate Program of Electro-Optical Engineering, National Taiwan Normal University, Taipei, Taiwan, C. W. Liu: Graduate School of Advance Technology, National Taiwan University, Taipei, Taiwan, T.-H. Hou, P. Su, M. H. Lee: Institute and Undergraduate Program of Electro-Optical Engineering, National Taiwan Normal University, Taipei, Taiwan

The classical memory device with cryogenic operation is in high demanded for quantum information processing. The cryogenic endurance of anti-ferroelectric (AFE) and ferroelectric (FE) $Hf_{1-x}Zr_xO_2$ capacitors is investigated for $\sim 10^{10}$ cycles (80 K). Moreover, the AFE capacitor exhibits a high speed response with $\sim$ 80% normalized switching $2P_{r,sw}$ for $t_p = 1$ μs compared to $\sim$ 60% for the FE capacitor at 80 K.

P9.EM - Multi Level Cell Reliability in Ge-Rich GeSbTe-Based Phase Change Memory Arrays, V. Meli, G. Navarro, J. Rottner, N. Castellani, S. Martin, N. P. Tran, G. Bourgeois, C. Sabbione, M. C. Cyrille: CEA, LETI, Université Grenoble Alpes, F-3800 Grenoble, France

In this paper we analyze the Multi-Level Cell (MLC) capability in Phase-Change Memory 4kb arrays based on Ge-rich GeSbTe alloys featuring high temperature data retention. Two Ge-rich alloys with a different amount of Ge are investigated and their MLC performances are compared with standard $Ge_2Sb_2Te_5$. Both Ge-rich materials feature a comparable data retention performance at 250°C in 1bit/cell mode, making them suitable for embedded automotive applications. Single pulse and Program-and-Verify MLC approaches are investigated to achieve 2 bits/cell. We compare the final distributions of the cell resistance levels and their evolution (drift) in time and in temperature. Finally, we show how the engineering of both materials stoichiometry and MLC programming strategy enable four distinguishable resistance levels even after one-hour bake at 150°C. These results prove MLC capability in Ge-rich GeSbTe PCM arrays.

P10.EM - Low-Frequency Noise Characteristics of Ferroelectric Field-Effect Transistors, Omkar Phadke, Khandker Akif Aabrar, Yuan-Chun Luo, Sharadindu Gopal Kirtania, Asif Islam Khan, Suman Datta, Shimeng Yu: School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA

Low-frequency noise (LFN) characterization of ferroelectric field-effect transistor (FeFET) is performed. Two types of FeFET are compared, one with oxide-channel (W-doped In_2O_3, i.e., IWO) compatible back-end-of-line (BEOL) process, and the other with silicon-channel using front-end-of-line (FEOL) process. The LFN measurements are performed for ON and OFF memory state of the devices to study the effect of polarization on the noise performance. Furthermore, the normalized noise power spectral density (NNPSD) value is extracted, and the IWO FeFET shows 5x lower value than the Si FeFET with a similar gate length. However, IWO FeFET has shown a 3x higher NNPSD than IWO MOSFET. The LFN experimental data is an indicator of the interfacial trap density. We conclude that the BEOL process eliminates the interfacial layer and reduces the trap density, while the ferroelectric gate stack induces more carrier fluctuation than the dielectric gate stack due to the polarization effect.

P11.EM - Monolithic 3D Integrated BEOL Dual-Port Ferroelectric FET to Break the Tradeoff between the Memory Window and the Ferroelectric Thickness, Om Prakash, Kai Ni: Rochester Institute of Technology, USA, Hussam Amrouch: Chair of Semiconductor Test and Reliability (STAR), University of Stuttgart, Germany

In this work, we applied the dual-port concept to decouple the trade-off between the Ferroelectric (FE) thickness (t_{FE}) scaling and Memory Window (MW) in the amorphous channel ferroelectric FET (FeFET) for monolithic 3D BEOL integration. To prove the effectiveness of the proposed device structure and explore design space, we developed a fully calibrated TCAD model and applied it to the amorphous channel FeFET study. We demonstrate the MW in two different scenarios: (i) write and read from the front gate, and (ii) write from the front gate and read

from the back gate. We show the t_{FE} and channel length scaling possibility in the second scenario, as well as the possibility for the multi-bit FeFET memory application.

P12.EM - A New Methodology to Precisely Induce Wake-Up for Reliability Assessment of Ferroelectric Devices, Tiang Teck Tan: Singapore University of Technology and Design (SUTD), 8 Somapah Road, Singapore 485999, Yu-Yun Wang: International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, Joel Tan: Singapore University of Technology and Design (SUTD), 8 Somapah Road, Singapore 485999, Tian-Li Wu: International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu, Taiwan, Nagarajan Raghavan, Kin Leong Pey: Singapore University of Technology and Design (SUTD), 8 Somapah Road, Singapore 485999

Studies on ferroelectric (FE) device degradation are performed on "woken up" devices. The process of waking up a device is typically done by applying a logarithmically increasing number of pulsed, alternating bipolar switching voltage cycles. However, this method has low resolution in precisely achieving the wake-up state, resulting in ambiguity in the current stage of the lifecycle of the device. Furthermore, ferroelectric device performance depends heavily on the spatio-temporal distribution of defects in the device stack, which are very different in the wake-up and fatigue phases of the life cycle. The standard bipolar pulsed stressing scheme as well as asymmetric device structure further complicate the analysis of the effects of voltage stressing on defect drift and subsequent device degradation. Here, we propose a new stressing methodology leveraging on an alternating stresssense scheme using CVS/RVS and positive-up-negative-down (PUND) waveforms to better control the extent of wake-up in the device. Wake-up and the associated changes to the spatiotemporal mapping of the charged defect concentrations can be more confidently ascertained using the proposed methodology, thereby enabling better understanding of the reliability physics governing wake-up and fatigue for FE devices in the future for lifetime prediction from accelerated life tests.

P13.EM - Reliability of InGaZnO Transparent ReRAM with Optically Active Pt-Nanodisks, Kavita Vishwakarma, Rishabh Kishore, Suman Gora, Mandeep Jangra, Arnab Datta: Department of Electronics & Communication Engineering, Indian Institute of Technology (IIT) Roorkee, Roorkee, Uttarakhand - 247 667, India

Reliability of a transparent Ag/indium-gallium-zinc-oxide (InGaZnO)/ITO ReRAM was assessed in terms of its dc-endurance and retention while InGaZnO contained optically active platinum nanodisks (Pt-ND) in it. It was observed that, λ =3D 500 nm can improve margin between HRS and LRS due to localized surface plasmon resonance (LSPR) that creates active surfaces on the Pt-NDs as suitable for chemical reduction of Ag^+ cations and growth of conductive filament (CF) under SET bias; LSPR also reduces HRS current due to localized electrons around the surfaces of Pt-NDs. On the contrary, CF was unstable during longer λ (700 nm) interaction with Pt-NDs, due to larger extinction cross sections of large diameter NDs that liberate more hot electrons through non-radiative channels preventing easy reoxidation/dissociation of CF under dc-cycles

P14.EM - Towards the Understanding of Ferroelectric-Intrinsic Variability and Reliability Issues on MCAM, Yishan Wu: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University & Peking University, China Department of Micro/Nano Electronics, SEIEE, Shanghai Jiao Tong University, Puyang Cai: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University & Peking University, China, Zhiwei Liu: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University & Peking University, China Department of Micro/Nano Electronics, SEIEE, Shanghai Jiao Tong University, Pengpeng Ren: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University & Peking University, China Department of Micro/Nano Electronics, SEIEE, Shanghai Jiao Tong University, Zhigang Ji: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiao Tong University & Peking University, China

The advent of hafnia-based ferroelectric field-effect transistors (FeFETs) prompted the evolution of data-intensive applications, such as multi-bit content addressable memories (MCAMs). Though the identification of FeFET variation sources and the understanding of FeFET retention problems have been discussed in existing literature, the impact of these issues on the FeFET-based MCAM is still not uncovered. Herein, we carried out the investigation on the variability and reliability issues of the FeFET-based MCAM. The threshold voltage (V_{th}) variation due to nonuniform ferroelectricity results in the long-tailed distribution of delay, thereby limiting the expansion of the MCAM array. The V_{th} shift during retention leads to the accuracy decline, which is more prominent after endurance cycling. Further optimization is required for the MCAM arrays to achieve more accurate and efficient search operation.

P15.EM - Full Reliability Characterization of Three-Terminal SOT-MTJ Devices and Corresponding Arrays, Xinyi Xu, Hongchao Zhang, Chuanpeng Jiang, Jinhao Li, Shiyang Lu, Yunpeng Li, Honglei Du, Xueying Zhang, Zhaohao Wang, Kaihua Cao, Weisheng Zhao: School of Integrated Circuit Science and Engineering, Beihang University, Beijing, China, Shuqin Lyu, Hao Xu, Bonian Jiang, Le Wang, Bowen Man, Cong Zhang, Dandan Li, Shuhui Li, Xiaofei Fan, Gefei Wang, Hong-Xi Liu: Truth Memory Technology Co., Ltd, Beijing, China

We have systematically investigated the reliability performance of spin-orbit torque (SOT) magnetic random access memory (MRAM) devices, including electromigration (EM), stress migration (SM), endurance and data retention. The results show that the SOT-MRAM devices pass the EM requirement over 10 years lifetime under the operation condition, and pass the SM requirement over 1000 hours baking at 175 °C. Moreover, high endurance close to 10^{14} cycles and robust data retention over 10 years storage time were demonstrated for the same SOT-MRAM devices. This full characterization fills the blank of SOT-MRAM reliability research and would contribute to the commercialization of the SOT-MRAM.

P16.EL - Multi-Finger Turn-On: A Potential Cause of Premature Failure in Drain Extended HV Nanosheet Devices, M. Monishmurali, Jatin, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India

The premature failure of a device under ESD stress causes the failure current to not scale with the number of fingers which is not desired. This work, for the first time, presents multi-finger turn-on as a potential cause of premature failure in multi-finger drain extended high voltage nanosheet devices. Detailed physical insights were developed into the multi-finger turn-on behavior. Further, the correlation with different device parameters has been used to find the cause for the non-uniform conduction in the device.

P17.EL - Extremely Large Breakdown to Snapback Voltage Offset (Vt1>>Vbd): Another Way to Improve ESD Resilience of LDMOS Devices, Aakanksha Mishra: Department of ESE, Indian Institute of Science, Bangalore, 560012, Karnataka, India;; Centre for Applied Research in Electronics, Indian Institute of Technology Delhi, New Delhi, India, B. Sampath Kumar, M. Monishmurali, Shaik Ahamed Suzaad, Shubham Kumar, Kiran Pote Sanjay: Department of ESE, Indian Institute of Science, Bangalore, 560012, Karnataka, India, Amit Kumar Singh: Semi-Conductor Laboratory, Mohali, Punjab, India, Ankur Gupta: Centre for Applied Research in Electronics, Indian Institute of Technology Delhi, New Delhi, India, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, 560012, Karnataka, India

Extremely large snapback voltage as an alternate way to improve the ESD robustness is proposed for the RESURF LDMOS devices which usually have low failure threshold. V_{t1}>>VBD is a "fail-to-protect" condition of the device which enables ESD protection to high-voltage power pins, expanding the ESD protection window for I/O applications. RESURF-implants in LDMOS result in lower I_{t1}, which is favorable for I/O devices with lower leakage. The effect of different LDMOS design approaches, load lines, and ESD stress duration on the V_{t1} is

systematically evaluated, using TLP experiments and 3D TCAD simulations. Finally, device design engineering guidelines are presented to achieve large V_{t1}, while developing physical insights into the underlying mechanisms.

P18.EL - Current Scalability Issues in Multi-Bank 5V PMOS ESD Structures: Root Cause and Design Guideline, Nagothu Karmel Kranthi: Analog Technology Development, Texas Instruments Inc., Bangalore, Karnataka, India, Yang Xiu, Yang Xiao: Analog Technology Development, Texas Instruments Inc., Dallas, Texas, USA, Rajkumar Sankaralingam: Analog Technology Development, Texas Instruments Inc., Dallas, Texas, USA

In this work, a unique Human Body Model (HBM) failure is presented in 5V-PMOS multi-finger structures. The failure is sensitive to the multi-bank layout, generally used to achieve higher holding voltage. Missing Transmission Line Pulse (TLP) failure current (I_{t2}) scalability is detected with pulse width, in multi-bank structures and a correlation is established with lower HBM failure. A detailed 3D-TCAD analysis approach is used to understand the PMOS turn-on in the single bank and multi-bank structures, in turn, the I_{t2} scalability for longer pulse width. The obtained insights are used to provide design guidelines for developing robust PMOS devices.

P19.EL - ESD Avalanche Diodes Degradation in EOS Regime, Vladislav Vashchenko, Hossein Sarbishaei; Analog Devices Corp, 130 Rio Robles, San Jose, CA, USA

Degradation of ESD avalanche diodes breakdown voltage (BV) characteristics in electrical overstress (EOS) regimes is observed and studied in BCD process technology. Both walk-in and walk-out effects are studied as a function of device structure parameters. It was shown that, in constant current avalanche stress regime, the level and direction of BV degradation can be controlled by changing the RESURF poly plate. High current breakdown TLP characteristics have been analyzed for the same phenomena

P20.EL - Engineering Custom TLP I-V Characteristic using a SCR-Diode Series ESD Protection Concept, Harsha B. Variar, Satendra Kumar Gautam, Ashita Kumar, Amogh K. M.: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy: Alpha & Omega Semiconductor, Sunnyvale, USA, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India

This work demonstrates an SCR-Diode series ESD Protection concept, which can be engineered to provide a custom TLP I-V characteristic. SCRs and diodes with dimensional variations have been used in different combinations and width ratios, which results in a range of TLP I-V characteristics. This protection circuit comes with several advantages as adaptability for various ESD protection windows, the benefits of using SCR as a protection device and the ease of designing the circuit. Along with TCAD studies, experimental data demonstrates that N-well and P-well doping of SCR can be used to further tune the Vhold and Ron of the protection circuit.

P21.EL - 3D Approaches to Engineer Holding Voltage of SCR, Satendra Kumar Gautam, Harsha B. Variar: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy: Alpha & Omega Semiconductor, Sunnyvale, USA, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India

Novel Silicon-Controlled-Rectifier (SCR) structures are experimentally demonstrated with the cathode and anode region engineering in the width (3D) plane. The engineering approach uses unique placements of P+ and N+ pockets/strips, instead of uniform anode/cathode implants. Experimental results show tunable holding voltages (3V - 10V) with high ESD failure current (I_{t2}) by using layout parameters related to the placement of these pockets/strips. The same has been demonstrated for over a dozen process lots. The physical insights and engineering guidelines into the holding voltage tuning has been explored using 3D process and device TCAD.

P22.EL - Characterization of Backside ESD Impacts on Integrated Circuits, Takuya Wadatsumi, Kohei Kawai, Rikuu Hasegawa, Kazuki Monta, Takuji Miki, Makoto Nagata: Graduate School of Science, Technology, and Innovation, Kobe University, Hyogo, Japan

Si-substrate backside of an integrated circuit (IC) chip becomes an open surface for electrostatic discharge (ESD) impacts in flip-chip assembly. This paper proposes an experimental framework for characterizing backside ESD impacts on test IC chips. An off-chip controllable high voltage pulse injector (HVPI) impacts flip-flop register files (FFs) as the on-chip victims. The HVPI produces a voltage spike with the peak amplitude up to 670 V and emulates spontaneous or intentional ESD occurrence. The voltage pulse with the height of 414 V induces bit flips among FFs when it is impacted on the Si backside and targeted around the cluster of FFs. The HVPI is held on an automated X-Y-Z stage and finely positioned on the Si backside. According to the physical layout of FFs with a total of 720 bits, the induction of bit flips is confirmed to be selective and localized.

P23.EL - Current Injection Effect on ESD Behaviors of the Parasitic Bipolar Transistors inside P+/N-Well Diode, Hui Wang, Pengyu Lai, Zhong Chen: Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, 72701, USA

The utilization of parasitic bipolar structures inside a typical P+/N-well as an additional electrostatic discharge (ESD) path is explored. The optimization on the lateral PNP (LPNP) is discussed. Device transmission line pulse (TLP) characterizations and technology computer aided design (TCAD) simulations by Silvaco have been performed to investigate the stand-alone LPNP ESD performance and effects of the base current injection on ESD behaviors of parasitic bipolar transistors.

P24.EL - TCAD study of the Holding-Voltage Modulation in Irradiated SCR-LDMOS for HV ESD Protection, Laura Zunarelli, Luigi Balestra, Susanna Reggiani: ARCES and Department of Electronic Engineering Guglielmo Marconi, Viale del Risorgimento 2, 40136 Bologna, Italy, University of Bologna Bologna, Italy, Raj Sankaralingam, Mariano Dissegna, Gianluca Boselli: Texas Instruments, 12500 TI Blvd, 75243 Dallas, TX

Abstract-This paper investigates a method to increase the holding voltage in a conventional Silicon Controlled Rectifier (SCR) for ESD power clamping. Specifically, a SCR-LDMOS device with 150 V trigger voltage and 9 V holding voltage is investigated assuming the application of high-energy electron irradiation. Based on previous experimental and TCAD investigations, the most relevant kind of defects is accounted for at different irradiation levels clearly showing an increase of the holding voltage up to 16 V without any other significant change in the TLP characteristics. The role of trapped charges in the holding regime has been addressed up to the thermal runaway through extensive numerical investigations.

P25.FA - Backside Failure Analysis of IGBT Power Devices Assembled in STPAK, E. Vitanza, C. Realmuto, M. La Marca, L. Torrisi: STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy

This paper addresses the problem of failure analysis of Insulated Gate Bipolar Transistor (IGBT) devices using a methodology free of artifacts, which can induce false behaviors, resulting from sample preparation. When an IGBT device fails in a non-catastrophic manner, usually high voltage values (V_{ces} >400V) must be applied to locate the fault/defect points; under these conditions, to avoid surface discharge, the front-side analysis cannot be applied, and the backside fault location approach becomes mandatory. When planning sample preparation, some constraints, peculiar to IGBT devices and crucial for their good performance, must be considered: the low thickness of the Si die and the p+ and n doped Si layers (field-stop) on the back side. The need to keep intact the Si bulk and the doped layers on the back side prompted the authors to abandon the standard method of sample preparation on the backside by drilling and mechanical polishing and to set up a specific safe methodology, which does not alter the electrical behavior of the device, making reliable and repeatable failure analysis possible.

P26.GaN - Evidence of Carbon Doping Effect on VTH Drift and Dynamic-RON of 100V p-GaN Gate AlGaN/GaN HEMTs, M. Cioni, G. Giorgino: Dipartimento di Ingegneria "Enzo Ferrari", University of Modena and Reggio Emilia, Via P. Vivarelli 10, 41125 Modena, Italy; STMicroelectronics, Stradale Primosole n. 50, 95121 Catania, Italy, A. Chini: Dipartimento di Ingegneria "Enzo Ferrari", University of Modena and Reggio Emilia, Via P. Vivarelli 10, 41125 Modena, Italy, C. Miccoli, M. E. Castagna, M. Moschetti, C. Tringali, F. Iucolano: STMicroelectronics, Stradale Primosole n. 50, 95121 Catania, Italy

The effect of the GaN buffer doping on V_{TH} drift and dynamic-R_{ON} of 100 V p-GaN gate AlGaN/GaN HEMTs is investigated in this work. Devices presenting two different Carbon (C) concentrations in the GaN buffer layer are characterized by means of vertical leakage, back-bias stress and off-state stress measurements. Back-bias stress on TLM structures is used to highlight the dynamics associated to C-related buffer acceptors. A significant difference is observed between samples with different C-doping, that correlates well with the different R_{ON}-degradation observed under conventional off-state stress conditions. Better V_{TH} and R_{ON} stability is observed on samples with less insulating buffer, highlighting the trade-off between leakage and dynamic performances of GaN power devices.

P27.GaN - Unique Dependence of the Breakdown Behavior of Normally-OFF Cascode AlGaN/GaN HEMTs on Carrier Transport through the Carbon-Doped GaN Buffer, Vipin Joshi, Sayak Dutta Gupta, Rajarshi Roy Chaudhuri, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India

Through this work, we report a unique reduction in the breakdown voltage of an AlGaN/GaN HEMT device when used in a cascode configuration. Detailed analysis reveals the breakdown voltage of the cascode HEMT to be a strong function of the carrier transport through the C-doped GaN buffer. A GaN buffer doping strategy is also proposed to improve the breakdown performance of the cascode HEMT device.

P28.GaN - Signatures of Positive Gate Over-Drive Induced Hole Trap Generation and its Impact on p-GaN Gate Stack Instability in AlGaN/GaN HEMTs, Rasik Rashid Malik, Vipin Joshi, Rajarshi Roy Chaudhuri, Mehak Ashraf Mir, Zubear Khan, Avinas N. Shaji, Madhura Bhattacharya, Anup T. Vitthal, Mayank Shrivastava: Department of ESE, Indian Institute of Science, Bangalore, Karnataka, India

In this work, we probe the physical mechanism responsible for V_{th} and gate current instability in p-GaN Schottky gated AlGaN/GaN HEMTs. Devices exhibited a negative V_{th} shift accompanied by a distinct increase in gate current, followed by gate failure, when driven at positive gate over-drives. Temperature and frequency dependent CV analysis is carried out along with capacitive-DLTS measurements to probe and validate the physical mechanism responsible for the observed gate instabilities. Generation of hole traps with an energy level of 0.43eV, in response to gate bias stress is found to trigger gate instability, subsequently leading to device failure.

P29.GD - Silicon Based Degradation Model for Various Types of Highly Integrated MOL Resistor Devices, A. Thiessen, M. Haack, M. Herklotz: FAB1 BEOL/MOL Reliability, Global Foundries Dresden, Wilschdorfer Landstraße 101, 01109 Dresden, Germany

An empirical resistor degradation model for various poly silicon and diffusion resistor types is derived from comprehensive silicon data. The power-law exponents imply that these resistor types exhibit degradation behavior typical of sub-diffusion, superdiffusion and normal diffusion, respectively. The degradation kinetic studies and TEM analysis indicate Ni diffusion as a dominant mechanism of the herein observed resistor degradation.

P30.GD - Polarity Dependency and 1/E Model of Gate Oxide TDDB Degradation in 3D NAND, Lina Qu, Shengwei Yang, Ming He, Rui Fang, Xiaojuan Zhu, Kun Han, Yi He: Yangtze Memory Technologies Co., Ltd., Wuhan 430205, China

1/E model is found more appropriate for gate oxide time dependence dielectric breakdown (TDDB) lifetime prediction in CMOS with 6.7 nm SiO_2 and poly electrode of 3D NAND technology, instead of widely used E model. It is believed that back-end-of-line process is the key factor contributing to the 1/E model, where hydrogen diffusion is originated from thick SiN and driven by final alloy. And anode hole injection (AHI) may be the dominant physic mechanism of this oxide degradation model. In addition, polarity dependency may be induced by decoupled plasma nitrogen (DPN) process and has no relation to 1/E model.

P31.GD - Machine Learning Based V-ramp VBD Predictive Model using OCD-Measured Fab Parameters for Early Detection of MOL Reliability Risk, Sungman Rhee, Hyunjin Kim, Sangku Park, Taiki Uemura, Yuchul Hwang: Quality Reliability Synergy, Samsung Electronics, Co.,Ltd., Hwa-seong si, Republic of Korea, Seungjin Choo, Jinju Kim, Hwasung Rhee, Shinyoung Chung: Samsung Foundry, Samsung Electronics, Co.,Ltd., Hwa-seong si, Republic of Korea

In this paper, we propose for the first time a breakdown voltage (V_{BD}) prediction method using structural parameters measured in-process for early detection of reliability risks in Middle-Of-Line (MOL). V_{BD} of the MOL is proportional to the distance of the Gate (PC) to Source/Drain-Contact (CA). Since PC to CA space can be calculated using MOL-related structural parameters at the early stage of the process, we created and validated models predicting V-$_{ramp}$ V_{BD} using five fab parameters measured in-process by optical critical dimension scatterometry (OCD). And we compared three modeling methods. The first is the geometrical calculation model (GCM), the second is multiple-linear-regression (MLR) method, and the last is the Multi-Layer Perceptions (MLP) model based on the machine learning (ML). We found the highest predictive consistency R^2 0.6 in ML method, and it is expected to contribute to the early prediction of MOL V-$_{ramp}$ V_{BD} through additional consistency improvements.

P32.GD - Polarity Dependency of MOL-TDDB in FinFET, Manisha Sharma, Hokyung Park, Yinghong Zhao, Ki-Don Lee, Liangshan Chen, Joonah Yoon, Rakesh Ranjan, Caleb Dongkyan Kwon: Samsung Austin Semiconductor, LLC, 12100 Samsung Blvd, Austin, TX 78754, USA, Hyewon Shim, Myung Soo Yeo, Shinyoung Chung: Samsung Foundry Business, Samsung Electronics, Korea, Jon Haefner: Samsung Austin Semiconductor, LLC, 12100 Samsung Blvd, Austin, TX 78754, USA

Stress polarity dependency of MOL-TDDB (Middle of Line-Time Dependent Dielectric Breakdown) is investigated on FinFET devices. Due to asymmetry in spacer dielectrics between Gate (PC) and Contact (CA), MOL-TDDB reliability can be different by bias polarity. From Vramp and TDDB evaluations, we observed MOL-TDDB reliability becomes worse when positive bias is applied to the CA side. Leakage current analysis and energy band diagram study suggested this reliability degradation can be explained by either more trap generation or more electron trapping in high-k layer (on PC side). This behavior can be suppressed by $V_{t-tuning}$ capping layer.

P33.MR - A Novel Data Recovery Technique for 3D TLC NAND Flash Memory using Intercell Program, Y. L. Chou, W. J. Tsai, G. W. Wu, W. Chang, T. C. Lu, K. C. Chen, C. Y. Lu: Macronix International Co., Ltd, No. 16 Li-Hsin Road, Science Park,. Hsinchu, Taiwan, R.O.C.

This paper proposes a novel data recovery technique based on an intercell program (IP) method to rescue the retention-failed data. When the error correction code (ECC) is unable to correct the read data owing to the retention loss by the lateral charge migration and vertical charge escape, the data recovery technique directly correct most of the errors in order that the remaining errors could be correctable by ECC. Neighboring wordlines are utilized to implement the IP operation to compensate for the retention loss. In addition, the neighboring wordlines can be used again after a partial erase operation. The proposed IP technique surpasses the word-line interference (WI) technique in various ways, such as data recovery capability, retention, and the erasable neighboring wordline.

P34.MR - Decomposition of Vertical and Lateral Charge Loss in Long-Term Retention of 3-D NAND Flash Memory, Jounghun Park, Gilsang Yoon, Donghyun Go, Donghwi Kim, Ukju An, Jongwoo Kim: Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea, Jungsik Kim: Department of Electrical Engineering, Gyeongsang National University, Jinju 52828, South Korea, Jeong-Soo Lee: Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea

For long-term retention characteristics of 3-D NAND flash memory, a method is proposed to decompose the measured V_T shift into several charge loss mechanisms, including lateral migration (LM), band-to-trap tunneling (BT), trap-to-band tunneling (TB), and thermal emission (TE). Based on the ΔV_T of the E-E-E pattern (EEE) at room temperature, the LM mechanisms of the P-E-P pattern (PEP) at high temperature (120 °C) are separated into the LM caused by hole (LMH) and electron (LME), respectively. Finally, the E-P-E pattern (EPE) and PEP are successfully decomposed into LMH, LME, TE, BT, and TB of trapped charges in the nitride layer. The proposed methodology is promising to quantitatively evaluate the charge loss mechanism in 3-D NAND flash memory.

P35.MR - A Physics-Based Model for Long Term Data Retention Characteristics in 3D NAND Flash Memory, Rashmi Saikia, Aseer Ansari, Souvik Mahapatra: Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, Maharashtra, 400076, India

Charge loss mechanisms during Data retention (DR) in GAA 3D NAND devices, Inter-cell charge loss of electrons in the Charge Trap Layer (CTL), and In-cell charge loss of electrons from tunnel oxide are modeled and analyzed using a physics-based Activated Barrier Double Well Thermionic Emission (ABDWT) model. The measured data retention characteristics for Solid Pattern (SP), of various distribution, sigma(σ) of the lower tail of the Cell Voltage Distribution (CVD) has been studied and modeled for various temperatures and programming levels (PL). Checkered pattern (CP) measured long-term data retention characteristics at various temperatures and program levels are modeled for both the loss components. 10 years projection is extrapolated across temperature and programing levels.

P36.MB - Reliability Improvement with Optimized BEOL Process in Advanced DRAM, J. H. Lee, B. W. Woo, Y. M. Lee, N. H. Lee, S. H. Lee, Y. S. Lee, H. S. Kim, S. Pae: Quality Assurance Team, Memory Division, Samsung electronics, 1-1, Samsungjeonja-ro Hwaseong-City, Gyeonggi-do, 18448, South Korea

Advanced DRAM with the reduced dangling bonds defects for the transistors could be manufactured by temperature control of passivation and optimizing BEOL process application. The decrease in passivation temperature increased hydrogen ion diffusion from the passivation layer. Passivation of the dangling bonds resulted in the increase of the retention time. Negative bias temperature instability (NBTI) of periphery device was relatively constant due to the pre-existing Si-H bonds. However, back end of line (BEOL) reliability showed drastic deterioration in time dependent dielectric breakdown (TDDB) and electro-migration (EM). Deterioration of Cu adhesion by water molecules and void formation was the main factor of drastic exacerbation of TDDB and EM lifetime. In order to strengthen the Cu adhesion, the optimized BEOL process was applied and the BEOL reliability was improved. As a result, the DRAM cell characteristic has been improved.

P37.MB - A Novel Methodology to Predict Process-Induced Warpage in Advanced BEOL Interconnects, Y. H. Lin, C. C. Lee: Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan, R.O.C., C. Y. Liao, M. H. Lin, W. C. Tu, Robin Chen, H. P. Chen, Winston S. Shue, Min Cao: Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, R.O.C.

Process-induced warpage caused by high-density interconnects in the back-end of line (BEOL) structure, may affect the performance and the reliability of the product during the packaging process. In this paper, a BEOL structure is used to develop a process-oriented simulation methodology to optimize the design and predict warpage. To reduce

simulation time and obtain accurate predictions, the equivalent material method and equivalent residual stress are used in our proposed method. The layer-by-layer warpage predictions matched the measurement data.

P38.MB - Impact of via Geometry and Line Extension on Via-Electromigration in Nano-Interconnects, A. S. Saleh: IMEC, Kapeldreef 75, B-3001, Leuven, Belgium; Department of Materials Engineering, Fac. Engineering Science, KU Leuven, B-3001, Leuven, Belgium, H. Zahedmanesh: IMEC, Kapeldreef 75, B-3001, Leuven, Belgium, H. Ceric: Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040, Wien, Austria, I. De Wolf: IMEC, Kapeldreef 75, B-3001, Leuven, Belgium; Department of Materials Engineering, Fac. Engineering Science, KU Leuven, B-3001, Leuven, Belgium, K. Croes: IMEC, Kapeldreef 75, B-3001, Leuven, Belgium

Via topology and line extension length can impact current crowding, stress distribution and void dynamics in the cathode region of nano-interconnects and therefore have an impact on electromigration lifetimes. In this study, a 2D physics-based model is employed to capture the effect of line extension and via taper angle on stress evolution and void dynamics, quantitatively. Varying via taper angle is shown to have higher impact on peak stress reduction (~0.8 MPa/nm of extra space) compared to line extension (~0.08 MPa/nm of extra space).

P39.MB - Stress Migration of Aluminum Backside Interconnect in Xtacking®, Kang Yang, Suhui Yang, Yan Ouyang, Shengwei Yang, Kun Han, Yi He: Yangtze Memory Technologies Co., Ltd., Wuhan 430205, China

Backside (BS) interconnects has shown significant advantages in 3D integral circuits for tackling the technology scaling induced frontside (FS) back-end-of-line (BEOL) routing congestion and RC delay challenge. As a representative BS interconnects architecture, Xtacking® 1.0 & 2.0 innovated by YMTC employs one Al metal layer at backside of memory cell wafer as BS interconnect routing for signal transfer. In this paper, we exploit the effect of silicon substrate to stress migration (SM) reliability of such Al BS interconnects, and offer several process approaches by film stack or film behavior optimization to improve SM performance of Al interconnects with the assistance of numerical simulation. An index of R_{SM} is proposed to reveal the statistic SM performance. Combining experiments and simulation result, a positive relationship is found between hydrostatic stress in numerical simulation and R_{SM}, and it brings a quantitative solution for SM in numerical simulation.

P40.NC - TID Response of an Analog In-Memory Neural Network Accelerator, B. Tolleson: School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85281 USA, C. Bennett: Sandia National Laboratories, Albuquerque, NM 87185-1084 USA, T. Patrick Xiao: Sandia National Laboratories, Albuquerque, NM 87185-1084 USA, D. Wilson: School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85281 USA; Sandia National Laboratories, Albuquerque, NM 87185-1084 USA, J. Short, J. Kim: School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85281 USA, D. R. Hughart, N. Gilbert, S. Agarwal: Sandia National Laboratories, Albuquerque, NM 87185-1084 USA, H. J. Barnaby, M. J. Marinella: School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ 85281 USA

A vector-matrix multiply (VMM) characterization chip was designed and fabricated in 350nm CMOS, including pulsers and a 10-bit analog to digital converter. The response of total ionizing dose (TID) was assessed using gamma radiation from a Cobalt-60 source. Inference was performed in situ during irradiation and VMMs computed by the accelerator were measured at increasing TID levels. Experimental results were used to create a circuit model, which was enabled a neural network accuracy simulation with CrossSim. Accuracy degradation on the CIFAR-10 task was a function of network architecture and was significantly reduced following >150 krad exposure.

P41.PK - Innovative Reliability Solution for WLCSP Packages, Klodjan Bidaj, Lauriane Gateka, Benjamin Ardaillon: STMicroelectronics, Imaging Division, 12, rue Jules Horowitz, 38019, Grenoble, France

This paper presents a reliability handling innovation for WLCSP product qualification. It improves reliability flow compared with standard chip board (CB) assembled WLCSP solutions. Evidence demonstrates that the concept works across a complete range of reliability stress conditions. Results with the new reliability proposal are confirmed to be similar to other standard CB solutions. This is verified through a full qualification plan on three diffusion lots using reliability trials under different environmental and bias conditions.

P42.PK - Demonstration on Warpage Estimation Approach Utilized in Fan-Out Panel-Level Packaging Enabled by Multi-Scale Process-Oriented Simulation, Chi-Wei Wang, Che-Pei Chang, Chang-Chun Lee: Department of Power Mechanical Engineering, National Tsing Hua University, Hsinchu, Taiwan 30013, R.O.C.

Despite of the enlarged area of the fan-out panel-level packaging (FO-PLP), the process-induced warpage may cause a serious yielding problem in the subsequent process and assembly for the package. The finite element analysis (FEA) is proposed in many researches to overcome the problem of time cost. The important issue is the discontinuous model and warpage after the sawing process from panel to strip, and strip to unit package for FEA. In this research, a redistribution layer (RDL) first FO-PLP is presented with integrated multiple scale of package model in FEA analysis. The equivalent materials method and the equivalent stress-free temperature in the process-orientation simulation is applied on RDL. The chemical shrinkage of molding underfill is also concerned. The multipoint constraint method is applied on the boundary of multiple scale model to solve the multiple scale problem with panel and strip. The warpage error between the simulation and experiment are below 10 %.

P43.PI - Insight into HCI Reliability on I/O Nitrided Devices, C. Doyen, V. Yon: ST Microelectronics, 850 rue Jean Monnet, Crolles, France., X. Garros, L. Basset, T. Mota Frutuoso: CEA-LETI, 17 Av. des Martyrs, Grenoble, France, C. Dagon, C. Diouf, X. Federspiel, V. Millon, F. Monsieur, C. Pribat, D. Roy: ST Microelectronics, 850 rue Jean Monnet, Crolles, France.

Hot carriers injection (HCI) degradation plays an important role in advanced technologies. We carried out an extensive analysis of this degradation mode on 55nm MOS transistors and showed that for large channel lengths, a stress at V_g =3D V_D becomes more critical than at V_g =3D V_{Gibmax} condition. This is imputable to an additional degradation mechanism distributed throughout the channel, which likely appears on nitrided samples.

P44.PI - Reliability Studies on Advanced FinFET Transistors of the Intel 4 CMOS Technology, M. Jamil, S. Mukhopadhay, M. Ghoneim, A. Shailos, C. Prasad, I. Meric, S. Ramey: Logic Technology Development Quality and Reliability, Intel Corporation, Hillsboro, Oregon 97124, U.S.A.

The Intel 4 CMOS FinFET technology delivers over 20% performance gains at iso-power over the prior generation (Intel 7). This paper reports reliability studies on the Intel 4 technology that demonstrate matched or better reliability while extending Moore's law in the areas of power, performance, and scaling over its predecessor. Industry-leading technology scaling comes with numerous challenges, including co-optimization of yield, performance, and reliability. This paper reports the development of Intel 4 technology with industry-standard reliability while delivering significant advancement in generational performance and density.

P45.PI - Impact of Process Variation on MIM Capacitor Lifetime, J. Melai, V. Subramanian, I. Pouwel: Front-End Innovation, CTO, NXP Semiconductors, Nijmegen, The Netherlands

MIM capacitor lifetime depends strongly on dielectric thickness. If there is significant spread in thickness this can make the TDDB lifetime estimation overly pessimistic. This can be countered by adapting the lifetime expression to include a metric for thickness. We have analyzed TDDB data in conjunction with measured capacitance density. This approach allows for more accurate lifetime estimates. It also facilitates process optimization choices.

P46.PI - Impact of Gate Stack Processing on the Hysteresis of 300 mm Integrated WS$_2$ FETs, L. Panarella: KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium; imec, Kapeldreef 75, Heverlee, 3001, Belgium, B. Kaczer, Q. Smets, D. Verreck, T. Schram: imec, Kapeldreef 75, Heverlee, 3001, Belgium, D. Cottt: KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium, D. Lin, S. Tyaginov, I. Asselberghs, C. Lockhart de la Rosa: imec, Kapeldreef 75, Heverlee, 3001, Belgium, G. S. Kart: KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium, V. Afanas'ev: KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium; imec, Kapeldreef 75, Heverlee, 3001, Belgium

The low quality of gate dielectrics deposited on 2D channels and the resulting poor reliability of 2D FETs are major issues that need to be addressed as a high priority. In this work, we compare 300 mm integrated dual-gate WS$_2$ FETs with two different interlayers (SiO$_x$ and AlO$_x$) in the top HfO$_2$-based gate stack by means of hysteresis measurements. The collected data enable the extraction of essential properties of defects in the gate oxide, which are commonly recognized as the main cause of instability of 2D FETs. In particular, the hysteresis width is evaluated as a function of the measurement sweep rate in order to investigate the time constants of the dominant defects in both interlayers. Finally, a new measurement-simulation scheme to extract the energy distribution of defects causing hysteresis is proposed. We observe that defects in AlO$_x$-capped devices have slower capture/emission time constants and much lower energy density approaching the conduction band minimum of the channel than those in SiO$_x$. Therefore, AlO$_x$ reduces hysteresis and improves reliability compared to SiO$_x$.

P47.PI - Enhanced DRAM Single Bit Characteristics from Process Control of Chlorine, Taiuk Rim, Kyosuk Che, Sehyun Kwon, Jin-Seong Lee, Jeonghoon Oh, Hyodong Ban, Jooyoung Lee: DRAM Product & Technology, Samsung Electronics Co. Ltd. 114 Samsung-ro, Pyeongtaek-City, Gyeonggi-Do, Korea

DRAM devices are scaling down for decades to get advantages on higher density and cost effectiveness, however it is becoming more challenging to sustain the same (or improved) product quality within smaller dimension and storage capacitance. In particular, when the size decreases, the increase in the electric field and the decrease in the storage capacitance is inevitable, so a new structure change or extreme control of impurities is required. Chlorine is one of the most commonly used chemical element in DRAM fabrication process such as the etching and the deposition, however it makes interface traps and increases single-bit failures such as the retention failure and the bit flip by the row-hammering. In this paper, the effect of chlorine on actual characteristics was studied by measuring chlorine concentration and analyzing electrical characteristics. To reduce the damage from chlorine, we suggested three strategies and verified their effectiveness: (1) blocking the chlorine diffusion, (2) reducing the initial chlorine concentration in the storage capacitors, and (3) outgassing the chlorine by chemical reaction. We believe that if new schemes are applied using the above strategies, single bit characteristics can be improved.

P48.PI - Voltage Acceleration of Power NLDMOS Hot Carrier Degradation, V. A. Vashchenko, H. Sarbishaei: Analog Devices Corp, 130 Rio Robles, San Jose USA

Hot carrier degradation (HCD) acceleration phenomenon by stress drain-source voltage of HV power NLDMOS devices have been studied using automated wafer level test methodology. A reasonable confidence level of the accelerated degradation rate prediction extrapolated from short term test results is demonstrated for the range of stress voltages between maximum operation voltage (MOV) and physical absolute maximum rating (AMR) determined through pulsed safe operating area (SOA). Two architectures of the HV power optimized NLDMOS devices are compared to LV NMOS. The applicability of high ~100x acceleration factor is demonstrated to enable full wafer data collection for statistical variation of the long-term reliability parameters for different wafer lots and device versions.

P49.PR - Analysis of SSD Acoustic Noise Generation Mechanism Depending on NAND Operation, Yusuf Cinar, Junghoon Kim, Eunho Oh, Sungki Lee, Changsik Kwon, Jonggyu Park: Solution Product & Development Team, Samsung Semiconductor, Hwaseong-si, Republic of Korea

This paper investigates the acoustic noise generation mechanism of solid-state drives (SSD) by analyzing NAND operation and measures variation of voltage, vibration, and acoustic pressure depending on the NAND operation. NAND operation is measured with respect to number of overlapped banks during its operation. It is observed that frequency components of bank interleaving process during the NAND operation affect voltage, vibration, and acoustic pressure variation. It was shown that acoustic noise of SSDs greatly depends on NAND operation.

P51.RE - Electrostatic Shielding of NAND Flash Memory from Ionizing Radiation, Matchima Buddhanoy, Biswajit Ray: Electrical and Computer Engineering Department, The University of Alabama in Huntsville, AL, 35899, USA

In this paper, we propose and experimentally evaluate an electrostatic shielding technique to protect the health of flash memory cells from ionizing radiation effects. The technique is based on pre-programming the memory module instead of irradiating it in the erase condition. We find that erased cells suffer more oxide degradation compared to programmed cells, suggesting pre-programming of memory modules before deploying in radiation-prone environments. We evaluate cell degradation by performing retention test on the irradiated memory chip which reveals significantly quicker charge loss for memory cells that were in the erased state during irradiation.

P52.RE - Write Recovery Time Degradation by Thermal Neutrons in DDR4 DRAM Components, Hyeongseok Oh, Myungsun Chun, Jiwon Lee: Department of Electronic Engineering, Hanyang University, 55 Hanyangdeahak-ro, Sangnok-gu, Ansan, Gyeonggi-do, 15588, South Korea, Shi-Jie Wen, Nick Yu: Cisco Systems Inc. 170 W. Tasman, San Jose, CA, USA, Byung-Gun Park: HANARO Atomic Energy Research Institute, Daejeon, Korea, Sanghyeon Baeg: Department of Electronic Engineering, Hanyang University, 55 Hanyangdeahak-ro, Sangnok-gu, Ansan, Gyeonggi-do, 15588, South Korea

In this study, a thermal neutron (TN) radiation test was conducted for DRAM devices of 1y nm technology. Accordingly, the write recovery time (t_{WR}) degradation was observed to range from 1-ns (degradation) to more than 15 ns (failure). Specifically, permanent timing degradation is expected, owing to secondary particles generated from the interactions of ^{10}B and TN. The samples from two manufacturers were compared and exhibited an 8.9 times maximum difference in the degradation cross-section.

P53.RE - Effects of Collected Charge and Drain Area on SE Response of SRAMs at the 5-nm FinFET Node, N. J. Pieper, Y. Xiong, D R. Ball: Department of ECE, Vanderbilt University, Nashville, TN, 37212 USA, J. Pasternak: Synopsys, Inc., Mountain View, CA, 94043 USA, B. L. Bhuva: Department of ECE, Vanderbilt University, Nashville, TN, 37212 USA

Single-port (SP) and two-port (TP) SRAM exposure to low-energy protons, alpha particles, and heavy-ions with varying supply voltages show particle linear energy transfer (LET) values and circuit design strongly influence charge collection, and subsequently SE cross-sections. Critical charge is not the dominant determinant of SE cross-section at the 5-nm node for all environments.

P54.RE - Radiation Hardened Flip-Flops with Low Area, Delay and Power Overheads in a 65 nm Bulk Process, Shotaro Sugitani, Ryuichi Nakajima, Keita Yoshida, Jun Furuta, Kazutoshi Kobayashi: Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology, Japan

We propose two types of radiation-hard flip-flops named PLTGFF and FBTIFF with low ADP (area, delay and power) overheads by increasing critical charge (Q_{crit}) at weak nodes. They have additional transistors and wires.

PLTGFF has the area, delay, and power overheads by 5%, 4%, and 10%, respectively. FBTIFF has the area, delay, and power overheads by 42%, 10%, and 22%, respectively. They were fabricated in a 65 nm bulk process. α-particle irradiation tests revealed that α-SERs of PLTGFF and FBTIFF were suppressed by 45% and by 90% than that of STDFF. By spallation neutron irradiation tests, neutron-SERs of PLTGFF and FBTIFF were suppressed by 18% and by 35% than that of STDFF. In the terrestrial environment, the proposed FFs have better trade-offs between reliability and performance than these of multiplexed FFs with large overheads.

P55.RE - Characterizing SEU Cross Sections of 12- and 28-nm SRAMs for 6.0, 8.0, and 14.8 MeV Neutrons,
Kazusa Takami, Yuibi Gomi: Dept. Communications and Computer Engineering, Kyoto University, Shin-Ichiro Abe: Nuclear Science and Engineering Center, Japan Atomic Energy Agency, Wang Liao: Photon Science Center, University of Tokyo, Seiya Manabe, Tetsuro Matsumoto: National Metrology Institute of Japan, National Institute of Advanced Industrial Science and Technology (AIST), Masanori Hashimoto: Dept. Communications and Computer Engineering, Kyoto University

This paper studies the characteristics of the single event upset (SEU) cross sections in 12- and 28-nm SRAMs induced by low-energy neutrons. Experimental results show that the SEU event cross sections of the 12-nm FinFET SRAM and 28-nm planar SRAM drop less significantly from 14.8 MeV to 6.0 MeV compared with 65-nm SRAM. This result shows that the importance of neutrons below 10 MeV elevates for terrestrial SER estimation for advanced SRAMs.

P56.RE - The Effects of γ Radiation-Induced Trapped Charges on Single Event Transient in DSOI Technology, Yuchong Wang, Siyuan Chen, Fanyu Liu, Bo Li, Jiangjiang Li, Yang Huang, Tiexin Zhang, Xu Zhang, Zhengsheng Han, Tianchun Ye: Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Institute of Microelectronics, Chinese Academy of Sciences, University of Chinese Academy of Sciences, Beijing, China, Jing Wan: State key lab of ASIC and System, School of Information Science and Technology, Fudan University, Shanghai, China

The effects of γ radiation-induced positive trapped charges in the top buried oxide layer (Q_{BOX1}) on the single event transient (SET) response of Double Silicon-On-Insulator (DSOI) transistors are examined for the first time through γ radiation and pulsed laser experiments. After γ radiation, a significant negative shift of threshold voltage for back-channel is observed for both DSOI NMOS and PMOS due to the Q_{BOX1}. The SET current was measured at the device level, and the SET current peak and full width at half maximum (FWHM) were calculated. The impact of Q_{BOX1} and back-gate bias on the SET current of the DSOI devices are analyzed in detail. The experiments demonstrate that the SET current of NMOS is enhanced due to the parasitic bipolar transistor (PBT) effect activated by Q_{BOX1}, which can be mitigated by applying a dynamic back-gate bias. However, the Q_{BOX1} inhibits the SET current and PBT for DSOI PMOS. TCAD simulations further validate this physical mechanism, and then the back-gate bias strategy is proposed for DSOI devices and circuits.

P57.RT - In-Product BTI Aging Sensor for Reliability Screening and Early Detection of Material at Risk,
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We have developed a new reliability monitoring suite, within a proprietary IP block that we call a CV® Core, with aging sensors embedded in the product layout and testable through the product I/O interface. We illustrate the application of the sensor suite with an example of the PMOS NBTI monitor, testable at the wafer level during product electrical wafer sort (EWS), as well after packaging at final test or during burn-in. During EWS, the wafer-level stress test can be used to identify a marginal chip, help material dispositioning for burn-in, or support additional

grading for chiplet matching for multi-chip modules. The aging sensors can also be used during the chip lifetime to monitor the device wear-out and alarm users about abnormal silicon aging rates against target mission profile. In this work, we show the wafer level test results for PMOS transistor degradation rates under NBTI stress, within wafer variability, and correlation of degradation rates between sensors stressed under different conditions.

P60.RT - Reliability Demonstration Testing Considering Multiple Failure Causes, Tobias Leopold: Faculty of Mobility and Technology, University of Applied Sciences Esslingen, Kanalstr. 33, 73728, Esslingen, Germany

Reliability Demonstration Tests (RDT) are a common procedure in reliability engineering to provide evidence of the minimum reliability achieved by a product [1]. Planning RDTs seems to be quite easy and the evaluation of the results can be done quickly based on the Binomial distribution. However, for most cases the assumption of distribution parameters of the failure behavior of the products has to be considered, especially when testing with a so called lifetime ratio. Another challenge is the presence of multiple failure causes.

P61.RT - Short-Flow Compatible Wafer-Level Reliability Assessment and Monitoring for PCM Embedded Non-Volatile Memory, Meindert Lunenborg: PDF Solutions SARL, Montpellier, France, Tomasz Brożek: PDF Solutions Inc., Santa Clara CA, USA, Laura Lorenzi: PDF Solutions Inc. Desenzano del Garda, Italy, Christoph Dolainsky: PDF Solutions GmbH, München, Germany, Violet Liu, Xiaoyi Feng: PDF Solutions Semiconductor Technology Co., Ltd, Shanghai, China

In this paper, we present newly developed, short-flow compatible, Phase-Change Memory (PCM) single bit cell monitors and their characterization, including wafer level reliability assessment through endurance cycling. The bit cells were embedded in specially designed mini-arrays based on the designs of 28nm FDSOI technology. Fast, highly parallel test with a proprietary test system and characterization with a range of optimized programming parameters was performed on PCM bit cells with different cell architectures and layout factors. Cell degradation including endurance cycling up to 10 million cycles was demonstrated for both short-flow and full-flow vehicles. In addition, the single bit structures were used in scribe-line monitors for WAT screening in the production environment.

P62.RF - Thermal and Statistical Analysis of Various AlN/GaN HEMT Geometries for Millimeter Wave Applications, N. Said: Material to System Integration laboratory, IMS, Talence, France; Systems Analysis and Architecture Laboratory, LAAS -CNRS, Toulouse, France, K. Harrouche, F. Medjdoub: Institute of Electronics, Microelectronics and Nanotechnology, IEMN -CNRS Lille, France, N. Labat: Material to System Integration laboratory, IMS, Talence, France, J. G. Tartarin: Systems Analysis and Architecture Laboratory, LAAS -CNRS, Toulouse, France, N. Malbert: Material to System Integration laboratory, IMS, Talence, France

Downscaling HEMT devices is nowadays substantial to allow their operation in the millimeter wave frequency domain. In this work, the electrical parameters of three different AlN/GaN structures featuring various GaN channel thicknesses were compared. After a DC electrical stabilization procedure, 96 HEMT devices under test exhibit a minor dispersion in DIBL and lag rates, which reflects an undeniable technological mastering and maturity. Evaluation of the sensitivity of devices with different geometries at temperatures of up to 200°C revealed that the gate-drain distance impacts R_{on} variation and not I_{dss} variation with temperature. We also showed that DIBL at moderate electrical field and the drain lags exhibit athermal behavior; unlike gate lag delays which can be thermally activated and exhibit a linear temperature dependence regardless of the size of the gate length and gate-to-drain distance.

P63.RF - GaN HEMTs Design and Modeling for 5G, Yueying Liu, John Wood, Zongyang Hu, Satyaki Ganguly, Jeremy Fisher, Mike Watts, Scott Sheppard, Don Gajewski, Basim Noori: Wolfspeed, Inc., Research Triangle Park, NC 27709, USA

As GaN on SiC technology becomes accessible to commercial users for 5G applications, modeling needs from transistor to system level has become a big challenge for designers. In this work we demonstrated the strategy of using multi-physics modeling for a high power GaN HEMT PA design to achieve the stringent design target goal on the product level. The simulation result shows excellent agreement between measurements and models. Meanwhile, to facilitate the design process at system level, behavioral modeling is used to predict module level performance by integrating models in complex signal scheme environment. The final product used with Wolfspeed's 5G targeted process with reliability test validity is demonstrated in the paper as well.

P64.TX - Self-Heating Aware Threshold Voltage Modulation Conforming to Process and Ambient Temperature Variation for Reliable Nanosheet FET, Sunil Rathore, Rajeewa Kumar Jaisawal, P. N. Kondekar, Navneet Gandhi: PDPM-IIITDM Jabalpur, India, Shashank Banchhor: IIT Roorkee, India, Young Suh Song: Korea Military Academy, Seoul, Korea, Navjeet Bagga: IIT Bhubaneshwar, India

Internal and external process variations severely affect the device threshold voltage (V_{th}) and, in turn, the device's reliability. For the first time, this paper presented a thorough analysis of the self-heating aware V_{th} variation of a Nanosheet FET and, thus, the device's aging. Using well-calibrated TCAD models, we evaluated the 'change in V_{th} and performed an extensive design space exploration to analyze: (i) the impact of work function (WF) modulation owing to metal grain sizes and effective grains (for confined dimensions) on V_{th} variation; (ii) the impact of ambient temperature (TA) on V_{th} variation; (iii) the influence of trap charges on device characteristics; (iv) how the consideration of RDF impacted V_{th}; (v) the device's aging, i.e., end of a lifetime (EOL). These investigations provided guidelines for designing a reliable Nanosheet FET (NSFET) to investigate and mitigate early aging.

P65.TX - The Effects of Process Variations and BTI in Packaged FinFET Devices, E. Bender: Department of Electrical and Electronic Engineering, Ariel University, Ariel 40700, Israel; Microsystems Technology Laboratories (MTL) Department, Massachusetts Institute of Technology, Cambridge, MA 02142, USA, J. B. Bernstein: Department of Electrical and Electronic Engineering, Ariel University, Ariel 40700, Israel, D. S. Boning: Microsystems Technology Laboratories (MTL) Department, Massachusetts Institute of Technology, Cambridge, MA 02142, USA

A correlation between device reliability and process variations in packaged devices is identified. Weibull distribution statistics are used in a novel method for finding the limit of precision possible for time-to-failure averaging. This study identifies increase of variance due to process variation with size scaling in three generations of technologies. There is a linear decrease in precision threshold which correlates to the size of the device. The results present a concern of BTI in technologies from 16nm and below.

P66.TX - The Correct Hot Carrier Degradation Model, J. B. Bernstein, E. Bender: Department of Electrical and Electronic Engineering, Ariel University, Ariel 40700, Israel; Microsystems Technology Laboratories (MTL) Department, Massachusetts Institute of Technology, Cambridge, MA 02142, USA, A. Bensoussan: Formerly EEE and Optoelectronics Expert Thales Alenia Space, Toulouse (France), now ReEExS Reliability Engineering Expertise Services

A model for the apparent negative activation energy that is observed when measuring hot carrier degradation has alluded the reliability physics community for several decades. The phenomenon is observed from changes in threshold voltage and mobility degradation and has been distinct from negative bias temperature instability (NBTI) in that the effect consistently increases with lower temperature. This effect is so consistent that an actual negative activation energy can be measured and has been reported from −0.1 to −0.4eV. We propose a model that considers the energetics of HCI that allows the mechanism to be modeled consistently for Silicon and GaN.

P67.TX - Excellent Reliability Performances of a Truly 5V nBOXFET for Automotive and IOT Applications,
D. Lipp, Z. Zhao, G. Krause, W. Arfaoui, E. Ebrard, G. Bossu, S. Evseev, M. Herklotz, M. Siddabathula: GlobalFoundries, Wilschdorfer Landstr. 101, 01109 Dresden, Germany

In a Fully-Depleted Silicon-on-Insulator (FDSOI) high-k metal gate technology a new device type is evaluated for 5V applications. To support high voltages, nBOXFET is using 20nm-buried oxide (BOX) as gate dielectric. Such a device fulfills the stringent requirements for 5V automotive and IOT applications. Hence, with the high operating voltage, it can be considered for voltage level shifter or DC-DC-converter design and compatible with still popular 5V standard supply. In this paper the improved TDDB and PBTI performance due to TCAD simulation motivated modifications of nBOXFET device is discussed. The excellent device reliability degradation performance from HCI point of view is presented as well as Plasma Induced Damage.

P69.TX - Atomic-Level Insight and Quantum Chemistry of Ambient Reliability Issues of the TMDs Devices,
Jeevesh Kumar, Hemanjaneyulu Kuruva, Harsha B. Variar, Utpreksh Patbhaje, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, Karnataka, 560012, India.

Long-term ambient reliability issues of the TMDs devices, like hysteresis behavior, are serious challenges to be addressed for its robust application. The root cause of the problem and the hypothesis presented earlier has not been inspected at the atomic level yet. This work presents the atomic-level insight into the vacancy-assisted interaction of TMDs with various ambient gases and its implications on the I-V hysteresis under different atmospheric, bias, and temperature conditions. The work reveals that introducing distinct donor and acceptor states is attributed to the adsorption of different atmospheric adsorbates over chalcogen defect sites in TMDs and their orbital interaction. The positive gate field ionizes donor states, resulting in a positive drain current shift (anticlockwise hysteresis loop), whereas the negative gate field ionizes acceptor states, leading to carrier recombination. The recombination phenomena are validated by demonstrating recovery of drain current shift when a strong negative gate bias was applied. The atomistic insights developed corroborates very well with the experimental observations.

P70.TX - The Impact of Back Bias, Strain and Hot Carrier Stress on The Random Telegraph Noise of Advanced SOI N-FETs,
Xinze Li, Qiao Teng, Ying Sun: School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China, 310000, Xiao Gong: Department of Electrical and Computer Engineering, National University of Singapore (NUS), 117576, Singapore, Sebastien Loubriat: CEA-LETI, MINATEC, 17 rue des Martyrs, F-38054 Grenoble Cedex 9, France, Guillaume Besnard, Christophe Maleville: SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France, Olivier Weber: STMicroelectronics, 850 rue Jean Monnet 38926 Crolles, France, Rui Zhang, Bing Chen, Dawei Gao, Ran Cheng: School of Micro-Nano Electronics, Zhejiang University, Hangzhou, China, 310000

In this work, the impact of hot-carrier (HC) induced degradation together with the effect of back bias (BB) on the random telegraph noise (RTN) in the SOI and tensile strained SOI n-FETs are investigated. It is found that the forward BB (FBB) can help to suppress the RTN of both the SOI and SSOI n-FETs with the former exhibiting larger improvement. Furthermore, as the ON time increases, n-FETs operated with FBB show less Id and RTN degradation as FBB pulls the carriers away from the top interface, reducing the occurrence of trapping/detrapping and the generation of interface defects over time. The effect of FBB and reverse back bias (RBB) on the RTN magnitude were explained by the change of carrier density distribution in the Si channel, according to the calibrated TCAD simulation results.

P71.TX - Effect of Precursor Defects in Oxide Layer on Ionizing Radiation Damage of Bipolar Junction Transistors,
Fengkai Liu, Lei Wu, Kai Wang, Enhao Guan, Xingji Li: School of Materials Science and Engineering, Harbin Institute of Technology, Harbin, China

The oxide-layer process temperature affects the intrinsic precursor defects of NPN bipolar junction transistors (BJTs). These defects cannot be characterized after manufacturing, while they can be characterized by radiation. In

this paper, the defect states, action forms, action effects on ionizing radiation damage, and the relationship between oxide-layer process temperature and defects are investigated. Based on the simulation and experiment results, a novel mechanism is proposed, which can illustrate the relationship between the oxide-layer process temperature and the precursor defects. That is, the higher the oxide-layer process temperature is, the more the deep-level defects are, the fewer the shallow-level defects are, and then the smaller the ionizing radiation damage is. This rule works at different hydrogen (H2) concentration. By means of studying the relationship between oxide-layer process temperature and precursor defects, it can help to remove the precursor defects and improve the quality of devices, and further provide ideas for radiation hardening.

P72.TX - Circuit Reliability of MoS$_2$ Channel Based 2D Transistors, Anand Kumar Rai, Harsha B. Variar, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, Karnataka, India, 560012

Inverters being the basic logic element of the circuits used, we have demonstrated MoS$_2$-based inverter degradation in terms of various parameters (inverter high output (V_{OH}), inverter low output (V_{OL}), rise time (t_r), gain) under critical stress conditions. These stress conditions include multiple voltage transfer characteristics (V_{TC}) sweeps, application of 10^4 pulses at the input of inverter (V_{IN}), change of output dynamic response with continuous pulses, and long duration DC stress for logic 0 and 1 at Vin. The percentage degradation in inverter characteristics was found to be increasing with an increase in supply voltage (V_{DD}) for all the stress cases. Among various stress cases run, Vol increased by 120 mV, Voh decreased by 150 mV, gain decreased by 500 mV/V, and tr increased by 4 µs. The degradation in inverter key parameters was found to be originated from the deterioration in the performance of the individual driver and load transistors.

P73.TX - Experimental Study of Self-Heating Effect in InGaAs HEMTs for Quantum Technologies down to 10K, F. Serra di Santa Maria, F. Balestra, C. Theodorou, G. Ghibaudo: Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC, Grenoble, 38000, France, C. B. Zota, E. Cha: IBM Research GmbH Zürich Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland

This work studies self-heating effects in InGaAs cryogenic HEMT devices, which aim at the enhancement of control/readout electronics performance in quantum computers. Starting from the well-known method of gate resistance thermometry, documented in literature for its reliable results, we characterized these devices down to deep cryogenic temperatures, namely 10 K, typical of signal-processing electronics for qubits, such as low-noise amplifiers (LNA). We furthermore compared the results with those belonging to far more industrialized silicon technologies (Si FDSOI and bulk), showing exceptional performance of the InGaAs HEMTs thanks to their lack of buried oxide and quantum well structure, which combined with their high electron-mobility, makes them a great study case for the technologies of the future.

P74.TX - Investigation on NBTI Control Techniques of HKMG Transistors for Low-Power DRAM Applications, Won Ju Sung, Hyun Seung Kim, Jung Hoon Han, Se Guen Park, Jeong-Hoon Oh, Hyodong Ban, Jooyoung Lee: DRAM Product & Technology, Samsung Electronics Co. Ltd., Pyeongtaek-City, Gyeonggi-Do, Korea

Conventional techniques for negative bias temperature instability (NBTI) improvement were evaluated to apply high-k metal gate (HKMG) for commercial DRAM applications. This research evaluated the role of several essential fabrication process on the PMOS employing channel SiGe (cSiGe) to contain NBTI. At the interlayer (IL), the RF nitridation (RFN) caused radical-induced re-oxidation, and capacitance equalized thickness (CET) increase. Then, reducing nitrogen (N) was not enough to refrain NBTI. On the other hand, modifying de-coupled plasma nitridation (DPN) on the high-k layer was effective to suppress threshold voltage degradation via NBTI with minimized transistor drain-induced barrier lowering (DIBL) degradation. Also, the research proves that the process

window of hydrogen (H) passivation must be optimized for low-power DRAM applications since the H passivation improved transconductance, but degraded NBTI.

P75.TX - OFF State Reliability Challenges of Monolayer WS₂ FET Photodetector: Impact on the Dark and Photo-Illuminated State, Rupali Verma, Utpreksh Patbhaje, Jeevesh Kumar, Anand Kumar Rai, Mayank Shrivastava: Department of ESE, Indian Institute of Science (IISc), Bangalore, India, 560012

This work reports the hot-hole injection-originated instability in the electrical characteristics (or the photodetection performance) of a monolayer WS_2 Field Effect Transistor (FET) photodetector. When a reverse bias (i.e., OFF-state bias or negative gate voltage) temporal stress with a lateral electric field is applied under visible light illumination, the photocurrent is found to vary with time by up to 1 to 2 orders of magnitude. Instability in the dark current is also observed post the stress under illumination, which is reflected in the variation in the transfer and the output characteristics of the FET. The observations impose severe limitations on the reverse-biased back-gated FET for sensitive photodetection applications using transparent single-layer WS_2 as the photoactive material.

P76.TX - Influence of Back Gate Bias on the Hot Carrier Reliability of DSOI nMOSFET, Xinyi Zhang, Kewei Wang: Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China; University of Chinese Academy of Sciences, Beijing 100049, China; Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing 100029, China, Fang Wang, Jiangjiang Li: Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China; Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing 100029, China, Zhicheng Wu: State key Lab of Fabrication Technologies for Integrated Circuits, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China; Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China, Duoli Li, Bo Li, Jianhui Bu: Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China; Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing 100029, China, Zhengsheng Han: Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China; University of Chinese Academy of Sciences, Beijing 100049, China; Key Laboratory of Science and Technology on Silicon Devices, Chinese Academy of Sciences, Beijing 100029, China

The hot carrier reliability under different back-gate bias in DSOI nMOSFET is studied. Reverse back-gate bias results in an over-all larger time exponents than the forward back-gate bias, which is attributed to the increased lateral electric field (as supported by TCAD simulation) and consequently a stronger interface state generation (related to SVE mechanisms). Such strong time acceleration is crucial for long term reliability prediction under circuit operation. The abnormal deviation among threshold voltage shift, linear/saturation drain current degradation is observed: through careful inspection of the degradation of the I-V characteristics, the competing role of the interface state generation and hot hole trapping is revealed, with a virtual channel shortening effect as supported by the increased DIBL values.

P77.TX - Investigation of Channel Dimension Dependence of BTI Degradation and Variation in Planar HKMG MOSFET, S. Q. Zhang, Y. S. Sun, D. Gao, H. Jiang, Z. Q. Yu, H. Zheng, J. L. Huang: Team of Design For Reliability, Hisilicon, Shanghai, P. R. China

Degradation induced by Bias Temperature Instability (BTI) and its variation of planar HKMG NMOS and PMOS transistors having various channel width, length and finger number are measured and analyzed. The BTI degradations of NMOS and PMOS show similar trends of channel length and finger number while different trends of channel width. The impact of channel length on BTI variation also shows a new observation. The physical mechanisms resulting in these performances are explained by combination of mechanical strain and number of defects. It's revealed that multi-finger is the prior choice than wider channel to enhance the drive capability of transistors.

P78.SiC - Carrot-Like Crystalline Defects on the 4H-SiC PowerMOSFET Yield and Reliability, B. Carbone, M. S. Alessandrino, A. Russo, E. Vitanza: STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy, F. Giannazzo, P. Fiorenza, F. Roccaforte: CNR-IMM, Strada VIII n. 5 - Zona Industrale, 95121, Catania, Italy

The correlation between the crystalline defectiveness and the fabrication yield and reliability of 4H-SiC in vertical PowerMOSFET is mandatory in order to fine tune the lifetime prediction for a specific mission profile. In particular, the vertical drain leakage current taken at the Electrical Wafer Sorting is usually used to overlap the electrical properties and the crystalline defects maps. This procedure ruled out any impact of the Carrot like defects standing alone on the 4H-SiC MOSFET reliability for the product under review. Carrot-like defects may play a role in the MOSFET reliability when they are combined with other crystalline or process defects.

P81.SiC - High Temperature and High Humidity Reliability Evaluation of Large-Area 1200V and 1700V SiC Diodes, In-Hwan Ji, Anoop Mathew, Jae-Hyung Park, Neal Oldham, Matthew McCain, Shadi Sabri, Edward Van Brunt, Brett Hull, Daniel J. Lichtenwalner, Donald A. Gajewski, John W. Palmour: Wolfspeed, Inc., 4600 Silicon Drive, Durham, NC, USA

For high power full SiC modules, the application requires highly reliable and robust 4H-SiC diodes in parallel with SiC MOSFETs. This work introduces new large size (50A rated) 1200V and 1700V 4H-SiC diodes which exhibit excellent performance under high temperature reverse bias (HTRB) and high voltage high temperature humidity (HV-H3TRB) conditions without sacrificing critical device performance such as forward voltage drop(Vf), Schottky Barrier height and ideality factor, and reverse leakage current. In this work, we have improved the device integration scheme for diode manufacturing, which enabled the successful completion of HTRB and HV-H3TRB qualification for automotive application.

P82.SiC - Investigation of Safe Operating Area on 4H-SiC 600V VDMOSFET with TLP and UIS Test Methods, Chao-Yang Ke, Yu-Chia Tsui, Bing-Yue Tsui, Ming-Dou Ker: Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

In high-power MOSFET, during the transient switching moment from on-state to off-state, it would suffer high V_{DS} voltage and high Ids current in a short period at the same time. Hence, safe operating area (SOA) is always an essential characteristic that must be considered when power modules were designed. It this study, two methods (TLP and UIS) to characterize SOA of a 600V vertical double-implanted MOSFET (VDMOSFET) fabricated by SiC process were performed. From the results of TLP measurement, it was found that the triggered voltage (V_{t1}) decreased with the increment of gate bias (V_{GS}). The snapback phenomenon was also observed in the TLP-measured I_{ds}-V_{ds} curve. To acquire the stable holding characteristic after VDMOSFET breakdown during UIS testing, a current-limiting resistance was used to prevent the device from burning out directly. Nevertheless, even though the device size of VDMOSFET was large enough (around 180k μm), it would still be burned out during the UIS testing with Vcc bias of only several hundred volts.

P83.SiC - Static, Dynamic, and Short-Circuit Characteristics of Split-Gate 1.2 kV 4H-SiC MOSFETs, Dongyoung Kim, Skylar DeBoer, Stephen A. Mancini, Sundar Babu Isukapati, Justin Lynch, Nick Yun, Adam J. Morgan, Seung Yup Jang, Woongje Sung: State University of New York Polytechnic Institute Colleges of Nanoscale Science and Engineering, 257 Fuller Rd, Albany, NY 12203

This paper reports static, dynamic, and short-circuit characteristics of split-gate (SG) 1.2 kV 4H-SiC MOSFETs. Conventional (C) MOSFETs and SG-MOSFETs were fabricated and evaluated. Identical conduction behaviors were achieved due to them having the same cell pitch. Although the maximum electric field in the gate oxide is higher in the SG-MOSFETs, this both device architectures obtained similar breakdown voltages with low leakage current. Due to the structure of the split-gate, the reverse capacitance (C_{rss}) was reduced by 32 % when compared

to conventional MOSFETs. As a result, switching loss for turn-on and turn-off transients was reduced, and thus total switching loss was reduced by 25 % in the SG-MOSFETs. Finally, the short-circuit (SC) ruggedness of the MOSFETs were evaluated. Even though the maximum drain current is higher in the SG-MOSFETs, under SC condition, a similar short-circuit withstand time (SCWT) was obtained. In order to further investigate short-circuit characteristics, non-isothermal simulations were conducted. It was discovered that there is no issue with the exposed edge of the gate in SG-MOSFETs under SC conditions despite the high electric field in gate oxide. Significantly reduced energy loss was achieved in the SG-MOSFETs with no compromise in static and short-circuit characteristics compared to the conventional MOSFETs.

P84.SiC - A Concise Electrothermal Model to Characterize the Thermal Safe-Operating Area of Power Transistor, Jian-Hsing Lee, Gong-Kai Lin, Chun-Chih Chen, Li-Fan Chen, Chien-Wei Wang, Shao-Chang Huang: Device Engineering Department, Vanguard-International Semiconductor Cop., Hsin-Chu City, Taiwan, Ching-Ho Li, Chih-Cherng Liao, Jung-Tsun Chuang, Ke-Horng Chen: Department of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, Hsin-Chu City, Taiwan

A physical model is derived to characterize the thermal safe-operating area (T-SOA) of power transistor. This model provides a concise methodology to get the precise and instant solutions of the temperature, and time to failure corresponding to IV for power transistor during the T-SOA measurement.

P85.SiC - Physical Insights into the DC and Transient Reverse Bias Reliability of ß-Ga_2O_3 Based Vertical Schottky Barrier Diodes, Harsh Raj, Vipin Joshi, Rajarshi Roy Chaudhuri, Rasik Rashid Malik, Mayank Shrivastava: Department of Electronic Systems Engineering, Indian Institute of Science (IISc), Bangalore, India

In this work, we report time-dependent breakdown of vertical ß-Ga_2O_3 Schottky barrier diodes (SBDs), even when stressed at voltages lower than the OFF-state breakdown voltage. Computational analysis revealed the process to be related to trapping induced field modulation. Further, novel anode contact scheme consisting of multiple field-plates and Schottky contact openings is proposed to mitigate this issue. The device structure thus fabricated demonstrated improved DC as well as transient reliability.

P86.SiC - SiC MOSFET Threshold Voltage Stability during Power Cycling Testing and the Impact on the Result Interpretation, Christian Schwabe, Xing Liu: Professorship of Power Electronics, Chemnitz University of Technology, Chemnitz, Reichenhainer Str. 70, Germany, Tobias N. Wassermann, Paul Salmen: Infineon Technologies AG, Max-Planck-Straße 15, 59581 Warstein, Germany, Thomas Basler: Professorship of Power Electronics, Chemnitz University of Technology, Chemnitz, Reichenhainer Str. 70, Germany

The gate-oxide processing for SiC MOSFET devices is challenging and can lead to pronounced trapping effects at the SiC/SiO_2 interface, which then can induce threshold voltage instabilities during switching and other long-term tests. This effect can influence the $R_{DS,on}$, if the channel is not completely closed, and also the temperature determination by the $V_{SD}(T)$ method. This paper presents a special measurement circuit for a live threshold voltage measurement during power cycling to study these issues during lifetime testing. The influence on the lifetime determination during power cycling is evaluated and can be in parts neglected for state-of-the-art devices. Even though high temperatures are present, the number of power cycles and respectively the time under a certain gate voltage is not sufficient to induce a reasonable gate threshold shift. For the investigated devices a negative influence on the lifetime testing and results interpretation can hence be ruled out.

P87.SiC - Reliability Comparison of Commercial Planar and Trench 4H-SiC Power MOSFETs, Shengnan Zhu, Limeng Shi, Michael Jin, Jiashu Qian, Monikuntala Bhattacharya, Hema Lata Rao Maddi, Marvin H. White, Anant K. Agarwal: Department of Electrical and Computer Engineering The Ohio State University, Columbus, OH, USA. (1)-(614)-787-5880, Tianshi Liu, Atsushi Shimbori, Chingchi Chen: Ford Motor Company, Dearborn, Michigan, USA

The gate oxide reliability, bias temperature instability (BTI), and short-circuit capability for commercial SiC power MOSFETs with planar and trench structures are evaluated and compared in this work. The asymmetric trench MOSFET has the thickest gate oxide among the tested devices, which provides the highest extrapolated gate oxide lifetime from the constant-voltage time-dependent dielectric breakdown (TDDB) measurements. Also, the asymmetric trench structure shows the longest short-circuit withstand time (SCWT) benefiting from the adjacent P^+ regions. However, the asymmetric trench MOSFETs show a high threshold voltage shift during the BTI measurements under AC stress, indicating more at or near SiC/SiO_2 interface defects. The double trench MOSFETs also show better short-circuit ruggedness, but no obvious advantages in the TDDB measurements and BTI results.

Thursday, March 30

Keynote 4
Thursday, March 30, 08:00 a.m. – 08:50 a.m. PDT
Venue: Regency Main

08:00 a.m.
KN4 (Keynote) - Building Reliability into the Modern Cloud, Rohit Vidwans; Ampere

As modern workloads move to the cloud at an unprecedented speed, Ampere's 80-core Ampere® Altra® and the 128-core Ampere® Altra® Max Cloud Native Processors are disrupting the status quo of legacy technology. Ampere is implementing a novel design methodology and state-of-the-art architecture to deliver reliable, high-quality, and consistent workload execution at the lowest possible power consumption and longer life expectancy. In his talk, Rohit will discuss the importance of reliability within these power-efficient multi-core designs, share some of the extensive testing and product qualification methodologies being implemented to address unique cloud-based core-utilization models and discuss other emerging challenges that Ampere will work with the industry to resolve in future products for the Modern Cloud.

Break
Thursday, March 30, 08:50 a.m. – 09:10 a.m. PDT

9A – RT (Reliability Testing & IRPS Late News)
Thursday, March 30, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency Main

09:15 a.m.
9A.1 - Customized Wafer Level Verification Methodology: Quality Risk Pre-Diagnosis with Enhanced Screen-Ability of Stand-by Stress-Related Deteriorations, Jiyoung Yoon, Bumgi Lee, Jaehee Song, Bokyoung Kang, Sangho Lee, Doh-Soon Kwak, Heonsang Lim, Ilsang Park, Jonghoon Kim, Sangwoo Pae: Memory Division, Samsung Electronics, Co.,Ltd., Hwa-seong si, Republic of Korea

This paper presents an accelerated stress of product at the wafer level for quality evaluations by performing pre-assessment of stand-by stress-related deteriorations. It is a customized defect-inducing evaluation methodology designed to have consistency with longer term package level test. The test was conducted on 18-nm 8Gb DDR4 DRAM wafers under various time and voltage stress conditions at elevated temperature to find the optimal condition for quality monitoring purpose. Then, the screen-ability was empirically verified through physical failure analysis and statistically verified through Fisher's Exact Test.

09:40 a.m.
9A.2 - A Detailed Comparison of Various Off-State Breakdown Methodologies for Scaled Tri-Gate Technologies, K. Joshi, D. Nminibapiel, M. Ghoneim, D. Ali, R. Ramamurthy, L. Pantisano, I. Meric, S. Ramey: Logic Technology Development Quality and Reliability, Intel Corporation, 2501 NW 229th Avenue, Hillsboro, OR 97124, USA

The source-drain punch-through current in off-state TDDB stress (OSS) is shown to significantly affect off-state breakdown behavior. This paper compares various OSS methodologies available in the literature and discusses how source-to-drain punch-through affects off-state breakdown and reliability. The proposed Drain-stress with Offset (DSO) OSS methodology limits punch-through to better reflect the actual field dependence of OSS breakdown for scaled tri-gate MOSFET technologies.

10:05 a.m.
9A.3 - Near Zero Field Magnetoresistance Spectroscopy: A New Tool in Semiconductor Reliability Physics, P. M. Lenahan: Engineering Science and Mechanics, The Pennsylvania State University State College, USA, E. B. Frantz, S. W. King: Intel Corporation Portland, USA, M. A. Anders: Broadcom Corporation, Bethlehem, USA, S. J. Moxim: National Institute of Standards and Technology, Gaithersburg, USA, J. P. Ashton: Keysight Technology, Santa Rosa, USA, K. J. Myers: Northrop Grumman, Falls Church, USA, M. E. Flatté: The University of Iowa, Iowa City, USA, N. J. Harmon: Coastal Carolina University, Conway, USA

A relatively simple addition to many widely utilized semiconductor device characterization techniques can allow one to identify much of the atomic scale structure of point defects which play important roles in the electronic properties of the devices under study. This simple addition can also open up the possible exploration of the kinetics involved in some reliability phenomena as well as in multiple transport mechanisms. This addition is a small (0 to a few milli Tesla) time varying magnetic field centered upon zero field. A readily observable difference between various device responses at zero and small fields can be observed in a wide range of measurements often used in semiconductor device characterization. These measurements include MOSFET charge pumping, MOS gated diode recombination current, so called DCIV measurements, deep level transient spectroscopy, simple current measurements in dielectric films and in pn junctions. Multiple materials systems of great technological interest can be explored with the techniques. They are based on near zero field magnetoresistance (NZFMR) phenomena, spin-based quantum effects involving magnetic field induced changes which occur in multiple electronic transport phenomena. Because these spin-based changes are strongly affected by fundamentally well understood spin-spin interactions such as electron-nuclear hyperfine interactions or electron-electron dipolar interactions, this NZFMR response has quite substantial analytical power. The NZFMR techniques can be gainfully applied to device structures based upon numerous materials systems, among them being silicon dioxide, silicon, silicon carbide, silicon nitride and amorphous SiOC:H films utilized in interlayer dielectrics.

9B – RE (Radiation Effect Reliability)
Thursday, March 30, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency I-II-III

09:15 a.m.
9B.1 - Fault Tolerant Frequency Synthesizers: From Charge-Pump PLLs to All-Digital PLLs (Invited), Qichao Ma, Gideon Adom-Bamfi, Adam Klekotko: Dept. Electrical Engineering (ESAT-ADVISE), KU Leuven, Belgium; CERN, Geneva, Switzerland, Venkata Sathyajith Kampati: Dept. Electrical Engineering (ESAT-ADVISE), KU Leuven, Belgium, Stefan Biereige: CERN, Geneva, Switzerland, Jeffrey Prinzie: Dept. Electrical Engineering (ESAT-ADVISE), KU Leuven, Belgium

This paper presents an overview of Single-Event Effects (SEEs) in Phase-Locked Loops (PLLs). Various sensitivity signatures in traditional charge-pump PLLs are introduced and corresponding circuit-level mitigation techniques are highlighted. The advantages of All-Digital Phase Locked Loops (ADPLLs) are identified and relevant circuit architectures are discussed, especially improvements related to the oscillator. Finally, SEEs in spiral on-chip inductors are shown, which are nowadays considered as a severe contributor to SEEs.

09:40 a.m.
9B.2 - Impact of Design and Process on Alpha-Induced SER in 4 nm Bulk-FinFET SRAM, Taiki Uemura, Byungjin Chung, Shinyoung Chung, Seungbae Lee, Yuchul Hwang, Sangwoo Pae: Device Solution, Samsung Electronics, Co., Ltd., Korea

This paper evaluates alpha-induced soft error rate (αSER) by alpha irradiation test in four different SRAMs and simulation. The test result shows the impact of three factors on αSER: process technology, the number of fins, and fin-pitch. The process technology advancing from 7 nm to 4 nm increases the αSER by 33%, the #fln change (2-fln to 1-fin) decreases the αSER by 54%, and the fin-pitch shrinking increases the αSER by 17% The simulation results show that the process variation does not contribute to the αSER. The BEOL thickness change can increase the αSER by 1.24×. This paper also discusses the αSER trend in SRAM from 130 nm to 4 nm technologies. Overall, the study aims to investigate the impact of process technology and design parameters on αSER in SRAMs.

10:05 a.m.
9B.3 - A 13-bit Radiation-Hardened SAR-ADC with Error Correction by Adaptive Topology Transformation, Yuya Aoki, Tatsuya Iwata: Graduate School of Engineering, Toyama Prefectural University 5180 Kurokawa, 939-0398, Imizu, Toyama, Japan, Takuji Miki: Graduate School of Science, Technology and Innovation, Kobe University 1-1 Rokkodai, 657-8501, Kobe, Hyogo, Japan, Kazutoshi Kobayashi: Graduate School of Science and Technology, Kyoto Institute of Technology Hashigami, 606-8585, Kyoto, Japan, Takefumi Yoshikawa: Graduate School of Engineering, Toyama Prefectural University 5180 Kurokawa, 939-0398, Imizu, Toyama, Japan

A 13-bit radiation-hardened-by-design (RHBD) successive approximation register ADC (SAR-ADC) has been proposed with almost no area overhead. The RHBD SAR-ADC has a differential topology with a couple of radiation detectors, and these radiation detectors are assigned, one for each of the differential data paths. The ADC transforms the topology adaptively from differential to single based on the result of radiation detection for error correction or reduction. Thanks to the error correction or reduction by the Adaptive Topology Transformation (ATT), measurement results show an order of magnitude improvement in cross-section and more than 10 dB SNDR enhancement under over 10^6 count/cm^2 irradiation condition.

9C – PI (Process Integration)
Thursday, March 30, 09:10 a.m. – 10:30 a.m. PDT
Venue: Regency IV-V-VI

09:15 a.m.
9C.1 - Impact of Barrier Metal Thickness on SRAM Reliability, Rakesh Ranjan, Pavitra Ramadevi Perepa, Ki-Don Lee, Hokyung Park, Peter Kim, Ganesh Chakravarthy Yerubandi, Jon Haefner: Samsung Austin Semiconductor, LLC, 12100 Samsung Blvd, Austin, TX 78754, USA, Caleb Dongkyun Kwon, Min-Jung Jin, Wenhao Zhou, Hyewon Shim, Shinyoung Chung: Samsung Foundry Business, Samsung Electronics, Korea

To understand the effect of barrier metal thickness (BM THK) of metal gate (MG) on static random access memory (SRAM) reliability, we evaluated 3 different wafer-level reliability (WLR) methods; random telegraph noise (RTN) characteristics (τ_c/τ_e, or capture/ emission time constant) and BTI recovery are studied on single-bit transistors, and SRAM static noise margin (SNM) degradation is also investigated with various stress configuration. Using three

different MG process splits, it is observed that RTN performance is modulated by BM THK. Through BM THK optimization, the best result (i.e., RTN↓, bias temperature instability (BTI) recovery↑, SRAM SNM shift↓) could be achieved, owing to less oxide damage by minimal trapping/de-trapping phenomenon. This clearly indicates the need of subtle process-reliability optimization. In addition, high temperature operating life (HTOL) is performed to confirm the SRAM Vmin shift at package-level test.

09:40 a.m.
9C.2 - Protection Schemes for Plasma Induced Damage from Well-Side Antennas, Hsi-Yu Kuo, Yu-Lin Chu: Quality & Reliability, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Hung-Da Dai, Chun-Chi Wang, Pei-Jung Lin: Product Engineering, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Ethan Guo: DRC, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Yu-Ti Su, Chia-Lin Hsu: ESD, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Kuan-Hung Chen: Product Engineering, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Tsung-Yuan Chen, Ryan Lu: Quality & Reliability, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Victor Liang: RD, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Kuo-Ji Chen: ESD, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C., Kejun Xia: Product Engineering, Taiwan Semiconductor Manufacturing Co., Ltd., 9, Creation Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300-77, R. O. C.

In this paper, several protection schemes for the plasma-induced damage (PID) from well-side antennas are proposed. The PID protection components made of diodes or ESD-like clamps are used to either balance the potentials between the wells or clamp the gate-to-source voltages of the victim gates. These protection schemes and the way to insert protection components have been verified by a variety of test structures designed in a 0.3μm BCD (Bipolar-CMOS-DMOS) process where NBL (N-type Buried Layer) is used as the isolation well.

Break
Thursday, March 30, 10:30 a.m. – 10:50 a.m. PDT

10A – TX (Transistors)
Thursday, March 30, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency Main

10:55 a.m.
10A.1 - GHz Cycle-to-Cycle Variation in Ultra-Scaled FinFETs: From the Time-Zero to the Aging States, Yiming Qu: School of Integrated Circuits, East China Normal University, Shanghai 200241, China; China Nanhu Academy of Electronics and Information Technology, Jiaxing 314001, China, Chu Yan, Xinwei Yu, Yaru Ding: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China, Yi Zhao: School of Integrated Circuits, East China Normal University, Shanghai 200241, China; College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; International Joint Innovation Center, Zhejiang University, Haining 314400, China

Through tremendous experimental data, this study focuses on the cycle-to-cycle variation (CCV) in ultra-scaled FinFETs at the GHz circuit speed, which is an urgent demand for the reliability community but has seldom been reported so far. The random occupancy of traps and interface states behind CCV was investigated with the different switching speeds and full $\{V_G, V_D\}$ bias space. Moreover, we observed the CCV degradation during hot carrier

degradation (HCD) and further explored its mechanism based on statistical datasets. This CCV study during HCD is helpful for the reliability variability-aware device/circuit co-design in advanced technology nodes.

11:20 a.m.

10A.2 - Investigation of Hot Carrier Enhanced Body Bias Effect in Advanced FinFET Technology, Zixuan Sun, Haoran Lu: School of Integrated Circuits, Peking University, Beijing 100871, China, Yongkang Xue: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiaotong University, Shanghai 200240, China, Wenpu Luo, Zirui Wang, Jiayang Zhang: School of Integrated Circuits, Peking University, Beijing 100871, China, Zhigang Ji: National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiaotong University, Shanghai 200240, China; Beijing Advanced Innovation Center for Integrated Circuits, Beijing 100871, China, Runsheng Wang, Ru Huang: School of Integrated Circuits, Peking University, Beijing 100871, China; Beijing Advanced Innovation Center for Integrated Circuits, Beijing 100871, China

In this paper, we observed non-negligible body bias effect after hot carrier degeneration (HCD) in 7 and 5nm FinFET technologies, even though they have negligible body bias dependence before HCD. We revealed that the trap-induced partial shift of the channel current towards the bottom of fin is the culprit for the enhanced body-biased effect, by combining TCAD and experimental results. We also studied mobility modulation by body bias effect before and after degradation. The results are beneficial for the reliability-aware circuit design against HCD particularly for FinFET-based circuits.

11:45 a.m.

10A.3 - Voltage Ramp Stress Test Optimization for Wafer Level Hot Carrier Monitoring in FinFET, Ri-an Zhao, Matthew Koskinen, Yang Liu, Xinggong Wan: GlobalFoundries, Malta, NY, 12020, USA

Inline voltage ramp stress (VRS) is used for fast wafer level reliability (fWLR) monitoring. For hot carrier injection (HCI) degradation, saturation current is monitored as drain and gate voltages are gradually increased. NFET VRS HCI is consistent with constant voltage stress (CVS) model, while PFET CVS model and VRS slope exhibits a large discrepancy. Similar to CVS data at short stress times and low gate voltage (V_g), the discrepancy is due to electron trapping during VRS when gate bias is less than drain voltage (V_d). As the gate voltage increases, the charge-trapping component reduces giving a better correlation for VRS slope versus the CVS model.

12:10 p.m.

10A.4 - New Insights on the Anomalous Cryogenic Random Telegraph Noise for 18 nm FDSOI CMOS, Ying Sun, Yuchen Gu, Junru Qu, Bing Chen: School of Micro-Nano Electronics, Zhejiang University, 310000, Hangzhou, China, Xiao Yu: Research Center for Intelligent Chips, Zhejiang Lab, Hangzhou 311121, China, Jing Wan: School of Information Science and Technology, Fudan University, Shanghai, 200438, China, Ran Cheng: School of Micro-Nano Electronics, Zhejiang University, 310000, Hangzhou, China, Genquan Han: School of Microelectronics, Xidian University, Xi'an 710071, China

In this work, cryogenic random telegraph noise (RTN) was characterized and investigated for 18 nm FDSOI CMOS. At 4 K, the noise characteristics are found to be more complicated than that at 300 K The effects of temperature and gate/drain biases on the drain current variation are extracted. A modified model based on the resonant tunneling model is proposed to explain the anomalous cryogenic RTN at different bias regions. Resonant tunneling and dissipative tunneling are dominant at different drain bias conditions, and coupling of the two mechanisms leads to a severe current fluctuation making it a more concerning factor in the cryogenic circuit design.

10B – NC (Neuromorphic Computing Reliability)
Thursday, March 30, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency I-II-III

10:55 a.m.

10B.1 - Reliability Assessment of Hafnia-Based Ferroelectric Devices and Arrays for Memory and AI Applications (Invited), L. Grenouillet, J. Barbot, J. Laguerre, S. Martin, C. Carabasse, M. Louro, M. Bedjaoui, S. Minoret, S. Kerdilès, C. Boixaderas, T. Magis, C. Jahan, F. Andrieu, J. Coignus: University Grenoble Alpes, CEA, LETI, Grenoble, France

Ferroelectricity in doped HfO_2 thin films was reported for the first time 12 years ago, generating strong interest in the non-volatile memory and logic community. Thanks to their CMOS compatibility and potential for scaling, hafnia-based Ferroelectric Random Access Memories (FeRAMs), Ferroelectric Tunnel Junctions (FTJs) and Ferroelectric Field Effect Transistors (FeFETs) are not only a breakthrough with respect to conventional perovskite-based ferroelectric (FE) devices but also potentially a revolution from an application prospective, in particular considering the non-volatility and intrinsic energy efficiency of these devices. However, their maturity is currently too low to consider practical applications. In this paper, we therefore focus on the reliability assessment of Metal/FE/Metal (MFM) and Metal/FE/Dielectric/Metal (MFDM) stacks, either in the form of large area ferroelectric capacitors, or in the form of kbit arrays integrated in CMOS Back-End of Line.

11:20 a.m.

10B.2 - Reliable FeFET-Based Neuromorphic Computing through Joint Modeling of Cycle-to-Cycle Variability, Device-to-Device Variability, and Domain Stochasticity, Simon Thomann, Albi Mema: Chair of Semiconductor Test and Reliability, University of Stuttgart, Germany, Kai Ni: Department of Microelectronic Engineering, Rochester Institute of Technology, USA, Hussam Amrouch: Chair of Semiconductor Test and Reliability, University of Stuttgart, Germany

Inherent domain stochasticity induced by the random spatial distribution of domains inside the ferroelectric (FE) layer along with Cycle-to-Cycle (CTC) and Device-to-Device (DTD) variability seriously hamper our ability to tune the FeFET threshold voltage (V_{TH}) towards the desired analog states required to realize neuromorphic computing. In this work, we present an framework that enables the joint modeling of Domain Stochasticity (DS), CTC, and DTD variability, through coupling TCAD models (accurately capturing the distributed channel of the underlying FET) with a multi-domain model that accurately captures the switching dynamics of the individual domains in the above FE layer. Hence, the hidden interaction between the spatial polarization fluctuation in FE and the distributed channel is unveiled. As a result, accurate modeling of V_{TH} distribution under various write scenarios is obtained. This, in turn, provides designers with guidelines on how analog states can be reliably programmed towards engineering reliable neuromorphic on unreliable FeFET.

11:45 a.m.

10B.3 - Reliability of Memristive Devices for High-Performance Neuromorphic Computing, Yue Xi, Xinyi Li: School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing China, Junhao Chen: Department of Physics, Tsinghua University, Beijing, China, Ruofei Hu, Qingtian Zhang, Zhixing Jiang, Feng Xu, Jianshi Tang: School of Integrated Circuits, Beijing Innovation Center for Future Chips, BNRist, Tsinghua University, Beijing China

With the rich internal ion dynamics, memristor-based neuromorphic computing emerges as a non-von Neumann computing paradigm to mimic biological neural networks and achieve high energy efficiency. However, to implement large-scale memristive neural networks, the reliability issue of memristive devices, including artificial synapse, dendrite, and soma, should be properly addressed. In this paper, recent works investigating the physical mechanisms and optimizations of memristive device reliability are presented. In particular, the relaxation effect of HfO_x-based artificial synapse is alleviated by using a ternary oxide as the thermal enhance layer, the device yield of TiO_x-based artificial dendrite is improved by proper material selection and interface engineering, and the device variability of NbO_x-based artificial soma is reduced by nitrogen doping. Furthermore, a bio-inspired dendritic neural

network with these three fundamental memristive devices is constructed and simulated to analyze the influence of device reliability. Using these optimized devices, the classification accuracy of the street-view house number dataset can be improved by up to ∼60%. The quantitative requirements of device reliability metrics are also provided as a guideline for future neuromorphic system design and implementation.

12:10 p.m.
10B.4 - Backhopping-Based STT-MRAM Poisson Spiking Neuron for Neuromorphic Computation, J. Tan: Singapore University of Technology and Design, 8 Somapah Rd, Singapore 487372; GLOBALFOUNDRIES Singapore Pte. Ltd., 60 Woodlands Industrial Park D St 2, Singapore 738406, J. H. Lim, J. H. Kwon, V. B. Naik: GLOBALFOUNDRIES Singapore Pte. Ltd., 60 Woodlands Industrial Park D St 2, Singapore 738406, N. Raghavan, K. L. Pey: Singapore University of Technology and Design, 8 Somapah Rd, Singapore 487372

Spin-transfer-torque magnetic random-access memory (STT-MRAM) is a proven technology for embedded non-volatile memory applications. The backhopping phenomena in STT-MRAM, whereby the resistance of the device oscillates under higher current, has been recently explored for emerging spiking neural network applications. We report a detailed characterization of backhopping in foundry compatible STT-MRAM having ∼15kb bit-cell arrays by analyzing the behavior of backhopping spike rate versus applied current and temperature. Our study shows that the backhopping in STT-MRAM exhibits the Poisson statistics with a controllable spike rate with current that displays three regimes: non-backhopping, exponential and linear. This mimics the behavior of a rectified linear unit (ReLU) neuron, a commonly used activation function in deep learning models. A spiking neural network (SNN) communication channel is simulated using the derived statistics and a first principles mathematical framework to analyze the reliability performance of backhopping-based SNN in terms of trading-off the accuracy and applied current.

10C – MR (Memory Reliability)
Thursday, March 30, 10:50 a.m. – 12:35 p.m. PDT
Venue: Regency IV-V-VI

10:55 a.m.
10C.1 - Reliability of 3D NAND Flash for Future Storage Systems (Invited), Akira Goda: Micron Memory Japan, Tokyo, Japan, Kishore Kumar Muchherla: Micron Technology Inc, San Jose, United States of America, Peter Feeley: Micron Technology Inc, Boise, United States of America

The 3D NAND Flash technologies have been successful, having realized the high density, high performance and highly reliable storage systems. With the continuous technology scaling, significant challenges and opportunities are expected in the future. SLC NAND technology plays a critical role for the high performance systems. The increased block size with further layer stacking requires innovative solutions to realize enhanced system performance and cost scaling. For the bits per cell (BPC) scaling beyond QLC, the reduction of the total cost of ownership (TCO) at the system level is the key. In this paper, we review and discuss the challenges and opportunities of 3D NAND reliability from the storage system perspectives.

11:20 a.m.
10C.2 - Insights into Device and Material Origins and Physical Mechanisms behind Cross Temperature in 3D NAND, Milan Pesic, Bastien Beltrando, Tommaso Rollo: Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, CA, USA, Cristian Zambelli: Dipartimento di Ingegneria, Università degli Studi di Ferrara, Ferrara, Italy, Andrea Padovani: DISIMI, Università di Modena e Reggio Emilia, Reggio Emilia, Italy, Rino Micheloni: Avaneidi srl, Saronno (VA), Italy, Rita Maji: DISIMI, Università di Modena e Reggio Emilia, Reggio Emilia, Italy, Lisa Enman, Mark Saly, Yang Ho Bae, Jung Bae Kim, Dong Kil Yim, Luca Larcher: Applied Materials Inc., 3050 Bowers Avenue, Santa Clara, CA, USA

Continuation of the scaling and increase of the storage density of the 3D NAND requires minimization and control of variability sources. Among the various reliability challenges, cross-temperature phenomena are considered as one of the reliability limiting factors of state-of-the-art 3D NAND devices. Starting from hypothesis that cross temperature effects are dominated by polycrystalline channel and retention loss at elevated temperature, we: (1) capture and quantify cell-to-cell variability sources within the Page; (2) provide first material and device driven insight (focusing on polyslicon) and its impact on cross-temperature along the Page and String and (3) link them with fail-bits of TLC-encoded 3D NAND.

11:45 a.m.
10C.3 - Depassivation of Traps in the Polysilicon Channel of 3D NAND Flash Arrays: Impact on Cell High-Temperature Data Retention, Mattia Giulianini, Gerardo Malavena: Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy, Luca Chiavarone: Process Research and Development Department, Micron Technology Inc., 20871, Vimercate, Italy, Alessandro S. Spinelli, Christian Monzio Compagnoni: Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, piazza L. da Vinci 32, 20133 Milano, Italy

In this paper, we report clear experimental evidence proving that programmed cells in a 3D NAND Flash memory array may experience an unexpected average increase in their threshold voltage (V_T) during high-temperature data retention. The phenomenon is explored as a function of the V_T level of the monitored cells, the string back-pattern, and the data-retention temperature. A physical picture is then proposed to explain its origin, which is traced back to the depassivation of some traps in the polysilicon channel of the 3D NAND strings. Results point out a new reliability issue to address and tackle in the design of next generation 3D NAND Flash technologies.

12:10 p.m.
10C.4 - Impact of Trapped Charge Vertical Loss and Lateral Migration on Lifetime Estimation of 3-D NAND Flash Memories, Y. H. Liu, T. C. Zhan, Y. S. Yang, C. C. Hsu, A. C. Liu: Phison Electronics Corp., Miaoli, Taiwan, W. Lin: Phison Electronics Corp., Miaoli, Taiwan; College of Artificial Intelligence, National Yang Ming Chiao Tung University, Hsinchu, Taiwan

In this work, a fundamental problem of the conventional temperature-accelerated life-test methodology is revealed owing to the coexistence of three failure mechanisms in 3-D NAND Flash memories. Different from previous studies, for the first time, we are able to separate the roles of trapped electron vertical loss and lateral migration experimentally in multiple bake temperature and different program/erase (P/E) cycle number without any simulation tool and fitting model according to the neighboring data pattern effect on threshold voltage (V_t) traces and the extracted activation energies (E_a) under various conditions. We found that V_t retention loss at lower temperatures tends to be dominated by trapped electron direct tunneling (DT) out from silicon nitride (SiN) to Si channel. At bake temperature rises, V_t loss in non-cycled cells is gradually originated from SiN trapped electron lateral migration via thermally assisted tunneling (ThAT) while V_t loss in P/E-stressed devices is mainly caused by trapped electron vertical escape from SiN storage layer through Frenkel-Poole (F-P) emission and the subsequent positive charge-assisted tunneling (PCAT) process.

Break
Thursday, March 30, 12:00 p.m. – 01:30 p.m. PDT

11A – SiC (Wide-Bandgap Semiconductors-SiC)
Thursday, March 30, 01:40 p.m. – 04:00 p.m. PDT
Venue: Regency Main

01:45 p.m.

11A.1 - Industrial Approach to the Chip and Package Reliability of SiC MOSFETs (Invited), Elena Mengotti, Enea Bianda, David Baumann, Gerd Schlottig, Francisco Canales: ABB Switzerland Ltd., Corporate Research Center, 5405 Baden-Dättwil, Switzerland

SiC-based power MOSFETs have become the major challengers for state-of-the-art Si technology in numerous power electronics applications. In ABB's portfolio, the list of examples includes motor drives, renewable energy conversion, battery energy storage systems and uninterruptable power supplies. The performance advantages of the wide-band-gap semiconductor are multiple and allow a clear size-to-cost benefit at the system level, making the introduction of SiC into selected products meaningful. To fully profit from the technology, the reliability level needs to be at least equivalent to the legacy Si-based solutions. However, the new technology requires new tests that address the relevant and novel failure mechanisms. The approach used by ABB is discussed in this paper. As part of the approach, various tests and exemplary results are presented, such as high voltage, high temperature tests, high dV/dt tests, avalanche ruggedness, repetitive surge current operation and dedicated gate oxide tests, as well as packaging related tests such as power cycling. The results show that manufacturers have gained control over some of the earlier limitations in first generation SiC devices, and that the available standards must evolve to reflect the SiC specific requirements compared to the previous semiconductor technology.

02:10 p.m.

11A.2 - The Concept of Safe Operating Area for Gate Dielectrics: The SiC/SiO$_2$ Case Study, P. Moens, F. Geenen, L. De Schepper, J. F. Cano, J. Lettens: Onsemi, Westerring 15, B-9700 Oudenaarde Belgium, S. Maslougkas, J. Franchi, M. Domeij: Onsemi, Isafjordsgatan 32C, 16440 Kista, Sweden

This paper introduces the concept of safe operating area (SOA) for the gate dielectric of SiC MOSFETs. The SOA is defined as the stress time=field=temperature space in which the transistor will remain within datasheet specifications and is a more useful parameter than the standardly reported time-to-failure (t_{fail}). Using Weibull statistics, the SOA at 5ppm, 20 Years, T=175°C is $\sim V_{gs}$=21.5V for onsemi SiC MOSFET products.

02:35 p.m.

11A.3 - Consideration on the Extrapolation of the Low Insulator Field TDDB in 4H-SiC Power MOSFETs, P. Fiorenza: CNR-IMM, Strada VIII n. 5 - Zona Industrale, 95121, Catania, Italy, F. Cordiano, S. M. Alessandrino, A. Russo, E. Zanetti, M. Saggio: STMicroelectronics, Stradale Primosole 50, 95121, Catania, Italy, C. Bongiorno, F. Giannazzo, F. Roccaforte: CNR-IMM, Strada VIII n. 5 - Zona Industrale, 95121, Catania, Italy

The gate oxide lifetime in 4H-SiC power MOSFETs is typically assessed at fixed and constant gate bias stress, monitoring the time-dependent dielectric breakdown (TDDB). In this work, the TDDB results obtained at three different insulator fields - either for positive and negative values - have been compared at wafer level. The TDDB was measured at 200 °C under the following conditions: (i) 3 (positive or negative) gate bias values; (ii) 3 (positive or negative) gate current values; (iii) 3 different insulator fields varying the gate bias stress voltage in each device after propaedeutic capacitance measurements to determine the gate insulator thickness. The three methods gave three lifetime prediction at low oxide field (under standard device operation). The physical explanation of these findings can be found, taking into account the device design across the source-body-JFET junction and the transient trapping phenomena at the SiO$_2$ interface.

Break
Thursday, March 30, 03:00 p.m. – 03:10 p.m. PDT

03:10 p.m.

11A.4 - Lifetime Modeling of the 4H-SĊC MOS Interface in the HTRB Condition under the Influence of Screw Dislocations, E. Van Brunt, D. J. Lichtenwalner, J. H. Park, S. Ganguly: Wolfspeed, Inc., 4600 Silicon Drive, Durham, NC, USA, J. W. McPherson: McPherson Reliability Consulting LLC, 2805 Shelton Way, Plano, TX, USA 75093

This work explores the lifetime model and failure modes of the 4H-SiC MOS interface in the depletion mode. Unlike accumulation mode TDDB, shorter lifetime and a strong defect dependence are observed in the depletion mode. The 1/E model is found to be a good fit for the observed TDDB lifetime data. Despite having a shorter lifetime than accumulation mode, the modeled lifetimes are sufficient for application deployment.

03:35 p.m.

11A.5 - Classification of Commercial SiC-MOSFETs Based on Time-Dependent Gate-Current Characteristics, E. Murakami, T. Takeshita, K. Oda: Department of Electrical Engineering, Kyushu Sangyo University, Fukuoka 813-8503, Japan, M. Kobayashi: Renesas Engineering Services Co., Ltd., Tokyo 187-8588, Japan, K. Asayama: JEOL Ltd., Tokyo 196-8558, Japan, Osaka University, Osaka 567-0047, Japan, M. Okamoto: National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba 305-8569, Japan

SiC-MOSFETs with high reliability have been desired for electric vehicles. We classify commercial SiC-MOSFETs into "heavily nitrided" and "lightly nitrided" based on time-dependent gate-current characteristics of fabricated devices. In "heavily nitrided" devices for higher mobility, high-voltage gate pulse for screening of B-mode (extrinsic defects) causes hole-trapping near the SiO_2/SiC interface through impact ionization. This phenomenon leads to an increase in gate current as well as a negative shift of threshold voltage. Moreover, this is enhanced at low temperatures (-60, $25°C$). Thus, high-temperature ($200°C$) screening is preferable. In addition, the relation between Weibull slopes for time-to-breakdown and charge-to-breakdown is closely examined.

11B – MB (Metallization/BEOL Reliability)
Thursday, March 30, 01:40 p.m. – 04:00 p.m. PDT
Venue: Regency I-II-III

01:45 p.m.

11B.1 - Towards Accurate Temperature Prediction in BEOL for Reliability Assessment (Invited), Melina Lofrano, Herman Oprins, Xinyue Chang, Bjorn Vermeersch, Olalla Varela Pedreira, Alicja Lesniewska, Vladimir Cherman, Ivan Ciofi, Kristof Croes, Seongho Park, Zsolt Tokei: Imec, Remisebosweg 1, 3001 Leuven, Belgium

Back end of line (BEOL) reliability strongly depends on the absolute temperature and temperature distribution in the interconnect lines. In this work, we present a holistic approach that combines experimental characterization, such as BEOL self-heating measurements and material properties characterization, with hybrid modeling to investigate the impact of BEOL design, materials, and technology options on the self-heating of the BEOL. The thermal coupling from Front End of Line (FEOL) to BEOL is also investigated in this work.

02:10 p.m.

11B.2 - Thermomigration-Induced Void Formation in Cu-Interconnects - Assessment of Main Physical Parameters, Y. Ding: Department of Materials Engineering, KU Leuven, Kasteelpark Arenberg 44, 3001, Leuven, Belgium; Imec, Kapeldreef 72, 3001, Leuven, Belgium, O. Varela Pedreira, M. Lofrano, H. Zahedmanesh: Imec, Kapeldreef 72, 3001, Leuven, Belgium, T. Chavez, H. Farr: QualiTau Inc., 5303 Betsy Ross Dr. Santa Clara, CA 95054, USA, I. De Wolf: Department of Materials Engineering, KU Leuven, Kasteelpark Arenberg 44, 3001, Leuven, Belgium; Imec, Kapeldreef 72, 3001, Leuven, Belgium, K. Croes: Imec, Kapeldreef 72, 3001, Leuven, Belgium

Using a dedicated test structure, the main physical parameters of void formation due to thermomigration (TM) were assessed. Based on physical and electrical void-analyses, we experimentally determined the time to void nucleation and estimated the heat of transport parameter $Q* = 0.21$ eV for Cu interconnects with CD$\sim$1 μm. Our studies show that TM has a 6x higher contribution to metal flux compared to the initial stress migration (SM) induced by the coefficient of thermal expansion (CTE) mismatch.

02:35 p.m.
11B.3 - Nickel Silicide Electromigration on Micro Ring Modulators for Silicon Photonics Technology, Brian T. McGowan: GlobalFoundries, U.S. Reliability Engineering, Essex Junction, VT, USA, Michal Rakowski: GlobalFoundries, Technology Development, Malta, NY, USA, Seungman Choi: GlobalFoundries, U.S. Reliability Engineering, Malta, NY, USA

Electromigration (EM) tests were performed on NiSi silicide heaters that are part of a photonic micro ring modulator (MRM). Measurement of the temperature kinetics of failure suggests an activation energy close to 2.0eV. Failure analyses confirm Ni migration is the failure mechanism. Reliability limits established by the EM tests combined with characterization of the MRM's temperature response quantifies the tradeoffs between device performance and reliability.

Break
Thursday, March 30, 03:00 p.m. – 03:10 p.m. PDT

03:10 p.m.
11B.4 - Effect of Frequency on Reliability of High-K Mim Capacitors, X. Federspiel, A. Griffon, M. Barlas, P. Lamontagne: Technology R&D, STMicroelectronics, 850 rue Jean Monnet 38926 Crolles, France

Dielectric relaxation phenomena in High-K capacitors have been reported to induce transitory effects. We present here a TDDB analysis including DC and pulsed DC stress applied on HK capacitors. We evidence a significant effect of frequency on TDDB. Using a model based on dielectric polarization dynamics, we found a good agreement with TDDB evolution with frequency but also a consistent behavior in terms of voltage acceleration factor as well as activation energy.

03:25 p.m.
11B.5 - Studying the Impact of Temperature Gradient on Electromigration Lifetime using a Power Grid Test Structure with on-Chip Heaters, Yong Hyeon Yi, Chris Kim: Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, USA, Chen Zhou: Nvidia, Santa Clara, CA, USA, Armen Kteyan, Valeriy Sukharev: Siemens EDA, Santa Clara, CA, USA

This work presents statistical data collected from 38 power grid test structures showing the detailed impact of temperature gradient on electromigration (EM) lifetime. The failure time, order, and location under different temperature gradients were compared to show that unexpected early EM failures can occur at temperature gradient regions due to accelerated tensile stress evolution inside the wire.

11C – PR (Product Reliability)
Thursday, March 30, 01:40 p.m. – 04:00 p.m. PDT
Venue: Regency IV-V-VI

02:10 p.m.
11C.2 - Towards Chip-Package-System Co-Optimization of Thermally-Limited System-on-Chips (SOCs), S. Mishra, V. Sankatali, B. Vermeersch, M. Brunion, M. Lofrano, D. Abdi, H. Oprins, D. Biswas, O. Zografos, G.

Hiblot, G. Van der Plas, P. Weckx, G. Hellings, J. Myers, F. Catthoor, J. Ryckaert: IMEC vzw, Leuven 3001, Belgium

Surge in compute-demand in consumer products, mobile phones, auto mobiles, datacenters for high performance computing (HPC) applications brings in major thermal challenges. This stems from growth in transistor density over the years and the associated power density increase. Advanced packaging techniques like 2.5D and 3D integration have a compounding effect. Hitting the thermal limits, not only affects the raw performance, power but also limits reliability of the product. Therefore, it has become necessary to foresee appropriate thermal solutions for target applications early in product development phase during thermal/power planning to assess viability of technology choices. In this paper, we assess the temperature distribution & anticipate cooling needs for future thermally-limited SOCs in advanced Angstrom nodes (A14 & A5). Thermal resistance breakdown from multiple sources is carried out to decouple contributions so as to explore possibility of a co-optimization of chip-package-cooling system. Some of the insights from our analysis could aid system software to do thermal aware job scheduling.

02:35 p.m.
11C.3 - Performing Machine Learning Based Outlier Detection for Automotive Grade Products, Y. L. Yang, P. C. Tsao, C. W. Lin, Ross Lee, Olivia Ni, T. T. Chen, Y. J. Ting, C. T. Lai, Jason Yeh, Arnold Yang, Wayne Huang, Peng Chen, Charly Tsai, Ryan Yang, Y. S. Huang, B. C. Hsu, M. Z. Lee, T. H. Lee, Michael Huang, Coming Chen, Liham Chu, H. W. Kao, N. S. Tsai: MediaTek Inc., Hsinchu, Taiwan

Near-zero defective parts per million (DPPM) and returned material authorization (RMA) from customers is the goal pursued by many companies. In this paper, a machine learning based method is proposed to detect outliers in the final test stage using the XGBoost algorithm and the Mahalanobis distance. We captured the weak integrated circuits (ICs) that passed the final test but failed in the system level test (SLT) or the verification of quality engineering aging (QEA). Compared to the random sampling, the experiments showed we could recognize $2\times \sim 3\times$ weak IC ratio in the SLT and $>10\times$ in the QEA to achieve automotive grade DPPM.

Break
Thursday, March 30, 03:00 p.m. – 03:10 p.m. PDT

03:10 p.m.
11C.4 - Development and Product Reliability Characterization of Advanced High Speed 14nm DDR5 DRAM with On-Die ECC, S. Lee, N.-H. Lee, K. W. Lee, J. H. Kim, J. H. Jin, Y. S. Lee, Y. C. Hwang, H. S. Kim, S. Pae: Memory Division, Samsung Electronics, Hwasung, Republic of Korea

The reliability characterization of fabricated 14nm DDR5 DRAMs with On-die Error Correction Code (ECC) and EUV process is presented for the first time. Intrinsic reliability of FEOL and BEOL WLR showed well above 10yrs of lifetime, 125°C. The products demonstrated no fails in high temperature operating lifetime (HTOL) of 1000hrs. The On-Die ECC design improved the single bit error rate by 10^{-6} times (refresh time $>4\times$). The failure rate, ppm of manufacturing burn-in process confirmed the healthiness of the baseline material and also effectively screen out and monitor any random defects. The presented 14nm DDR5 DRAMs are well in production for the PC segments and have been shipping and qualified for the Server segments.

Break
Thursday, March 30, 04:00 p.m. – 04:20 p.m. PDT

Closing Ceremony, Prize Drawing & 2024 Introduction
Thursday, March 30, 04:20 p.m. – 04:35 p.m. PDT
Venue: Regency Main